Sheet 7

1) Implement the following function using suitable multiplexer
   $F(A, B, C, D) = \sum(0, 3, 5, 6, 8, 9, 14, 15)$
   Ans: 8x1 mux (the number of its selection lines equals the number of input variables - 1): A, B and C on selections and D on inputs as follows:
   I0= D', I1= D, I2= D, I3= D', I4= 1, I5= 0, I6= 0 and I7= 1

2) Implement the full subtractor using suitable multiplexers.
   Ans: for the truth table of the full subtractor use two 4x1 muxs one for B borrow and one for D difference.

3) Construct a 4x16 decoder from 2x4 decoders.
   Ans: 5 decoders will be used, 4x16 decoder has 4 inputs. So the two least significant inputs will be inputs for 4 decoders, while the first two inputs will be the input of the fifth decoder whose outputs are connected to the enables of the other four decoders.

4) Construct a 8x1 multiplexer from 4x1 multiplexers and one 2x1 multiplexer.
   Ans: 8x1 mux has 3 selectors, the two least significant bits will be selectors for two 4x1 muxs and the outputs of these muxs wills be inputs to 2x1 mux whose selection is the most significant remaining bit.

5) Implement practically a full adder using a suitable NAND decoder.
   Ans: 3x8 decoder and two NAND gates for C and S

6) Implement practically the following function using a suitable multiplexer
   $F(W, X, Y, Z) = \sum(0, 1, 3, 4, 8, 9, 15)$
   Ans: 8x1 mux: W, X and Y on selections and Z on inputs as follows:
   I0= 1, I1= Z, I2= Z', I3= 0, I4= 1, I5= 0, I6= 0 and I7= Z

Good Luck
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