Faculty of Computer & Information Sciences
Ain Shams University
**CHW 261: Logic Design**
Tutorial Sheets 2020-2021
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# Tutorial 5

1) How the three-input NAND can be expanded using two-input NAND?
2) Simplify the following Function and then implement it using 2-Level NAND gates only?
    a. F(A, B, C, D) = ( 5, 6, 7, 8, 13, 14, 15)
3) Draw the multiple-level NAND circuit for the following expression:
    a. F(w,x,y,z) = w(x + y + z) + xyz
4) How the 3-inputs NOR can be expanded using two-input NOR?
5) Simplify the following Function and then implement it using 2-Level NOR Gates only?
    a. F (W, X, Y, Z) = ( 0, 2, 4, 5, 8, 9, 10, 14), d (W, X, Y, Z) = (1, 6, 13)
6) Draw the multiple-level NOR circuit for the following expression:
    a. F(A,B,C,D) = CD(B + C)A + (BC' + DE')
7) Design an odd Parity generator \parity checker circuits.