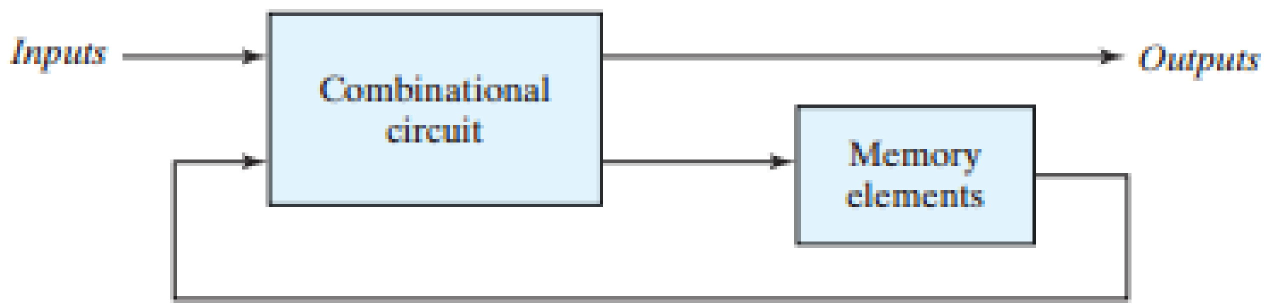
Digital Design

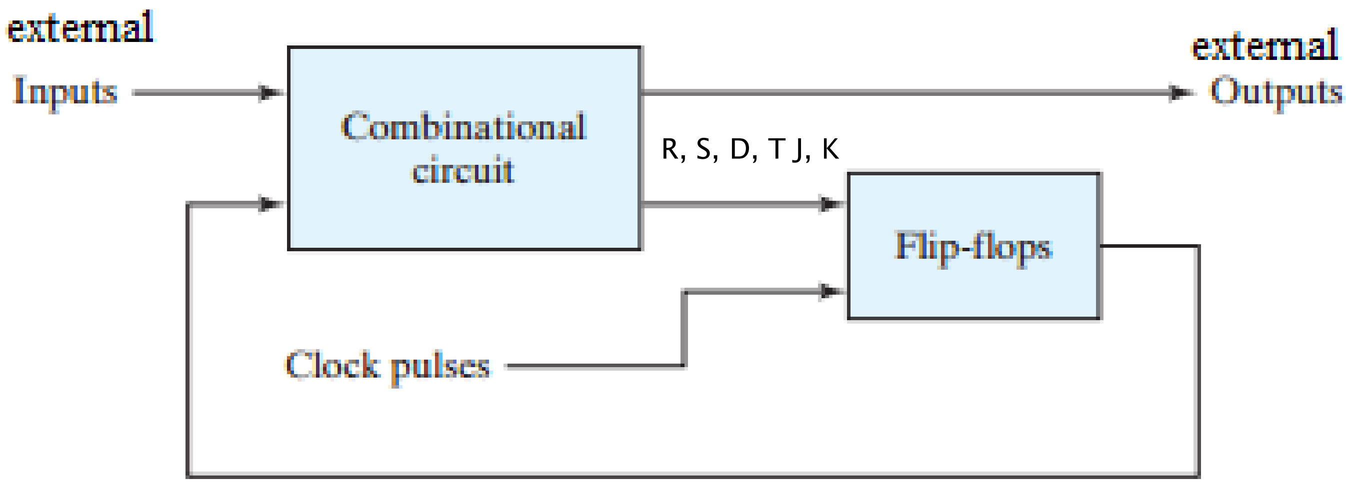
Lecture of week 10

Dr Manal Tantawi

Recap: Synchronous Sequential Circuits



Recap: Synchronous Sequential Circuits



Recap: Synchronous Sequential Circuits

Design Procedure

1) State Diagram

2) Number of ex. Inputs and outputs and number of flipflops

3) State Table

4) Simplified expressions using Kmap for external outputs and inputs of flipflops

5) Logic diagram

Designing using JK flip flops (deriving Excitation Table)

1) Qn= 0 -> Qn+1 = 0

0 ->0

J	K
0	0
0	1
0	**X**

JK Flip-Flop

J	K	Q(n + 1)	
0	0	$Q(n)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(n)$	Complement

2) Qn= 0 -> Qn+1 = 1

0 ->1

J	K
1	0
1	1
1	**X**

3) Qn= 1 -> Qn+1 = 0

1 ->0

J	K
0	1
1	1
X	**1**

4) Qn= 1 -> Qn+1 =1

1 ->1

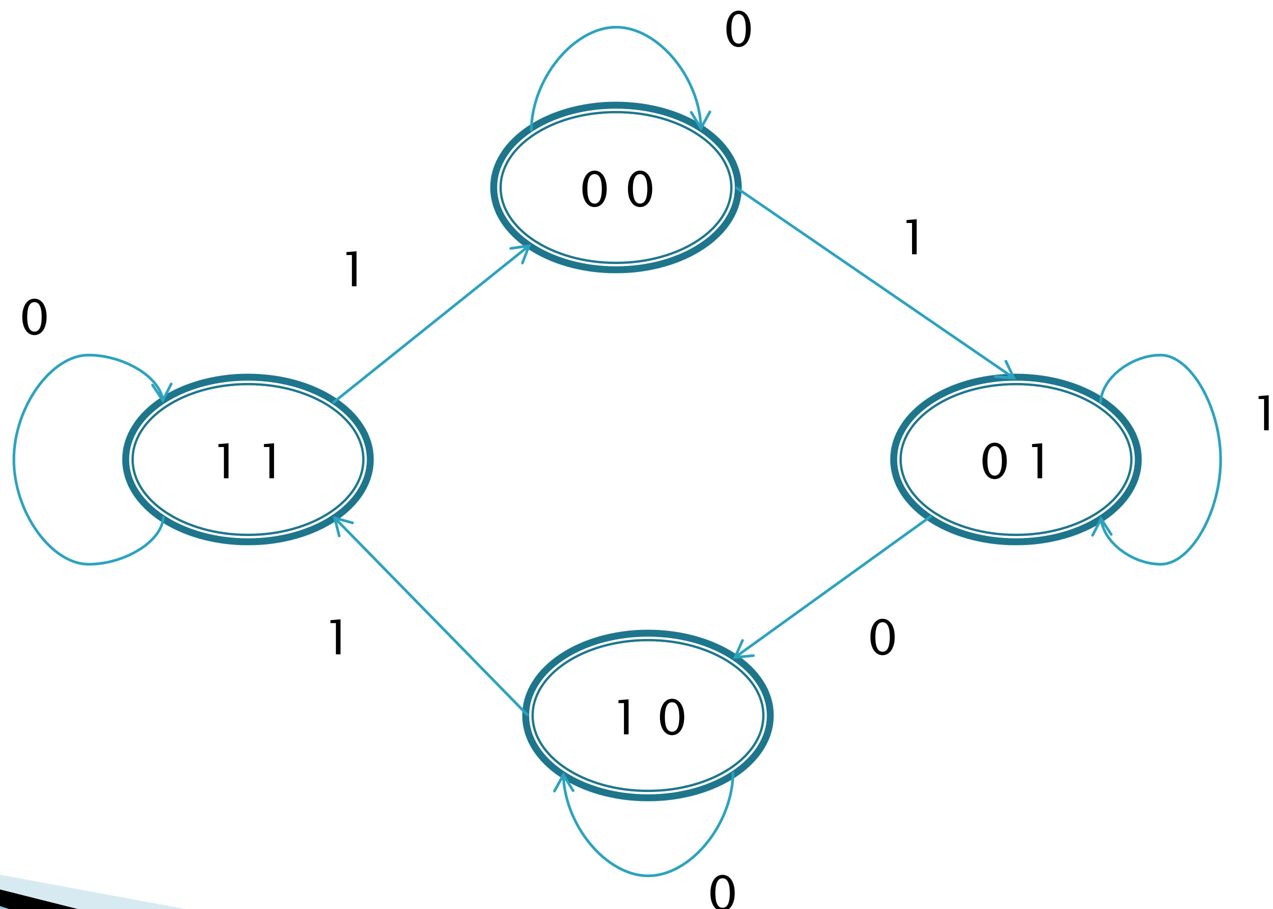
J	K
0	0
1	0
X	**0**

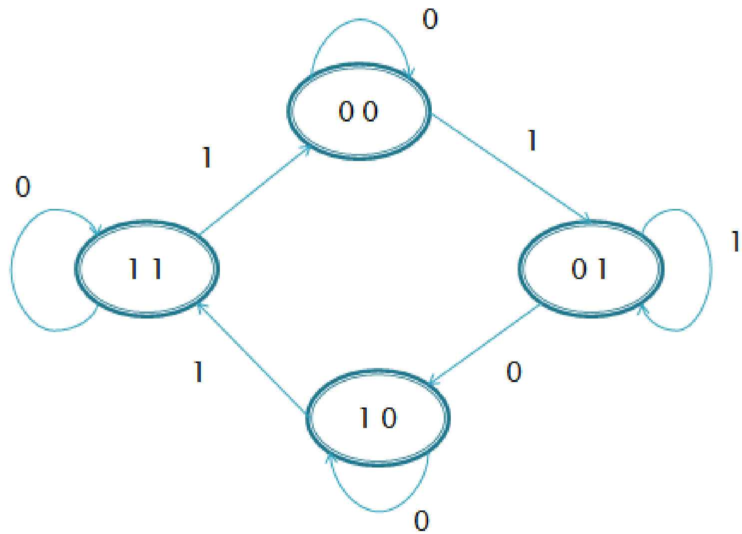
Designing using JK flip flops (deriving Excitation Table) continued..

$Q(n)$	$Q(n+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Flip-Flop

Design a sequential circuit with input x that follows the following state diagram using JK flip flops



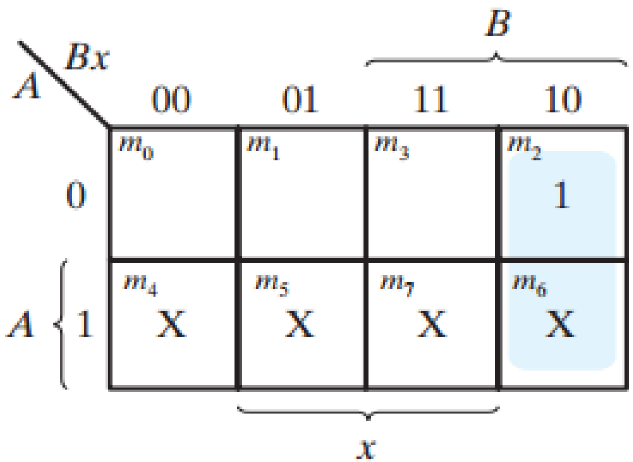


Q(n)	Q(n + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

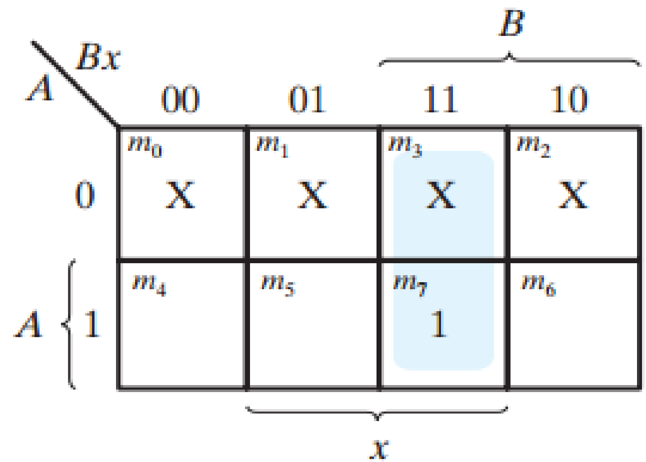
JK Flip-Flop

Present State		Input	Next State		Flip-Flop Inputs			
A	*B*	*x*	*A*	*B*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

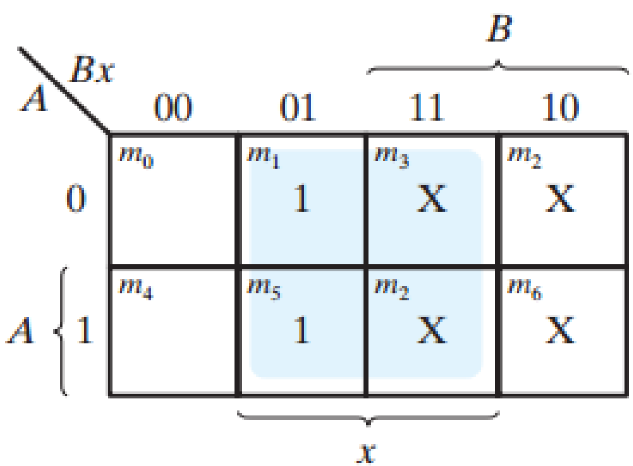
3)



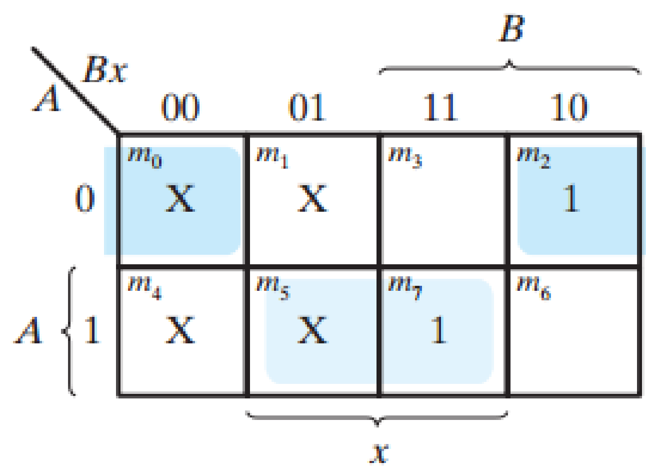
$J_A = Bx'$



$K_A = Bx$

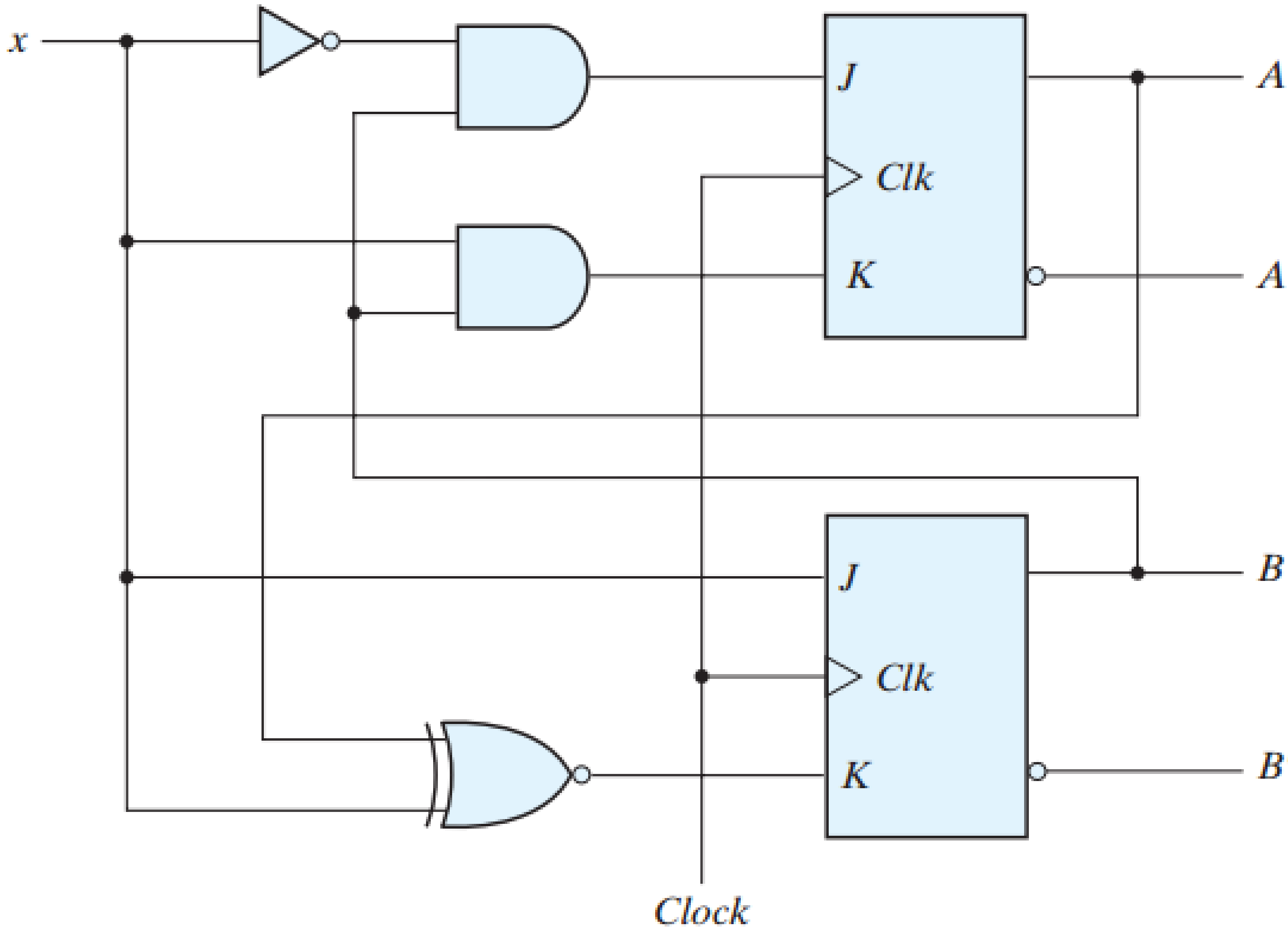


$J_B = x$

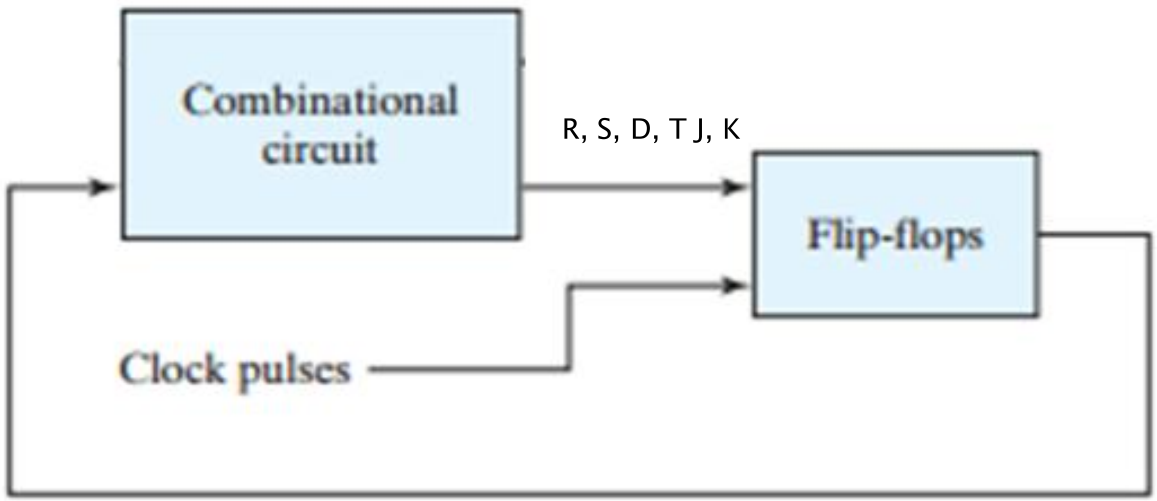


$K_B = (A \oplus x)'$

4)

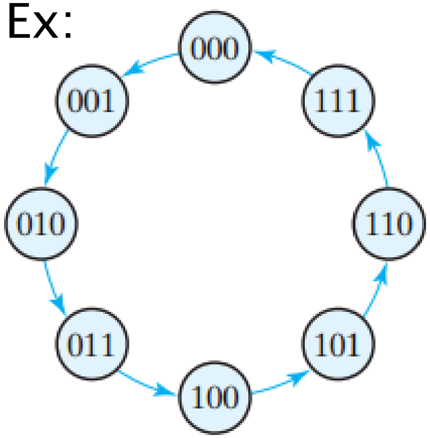


Counters



Combinational circuit
R, S, D, T J, K
Flip-flops
Clock pulses

Ex:



000
001
010
011
100
101
110
111

Design a 2 bit counter using JK flip flops

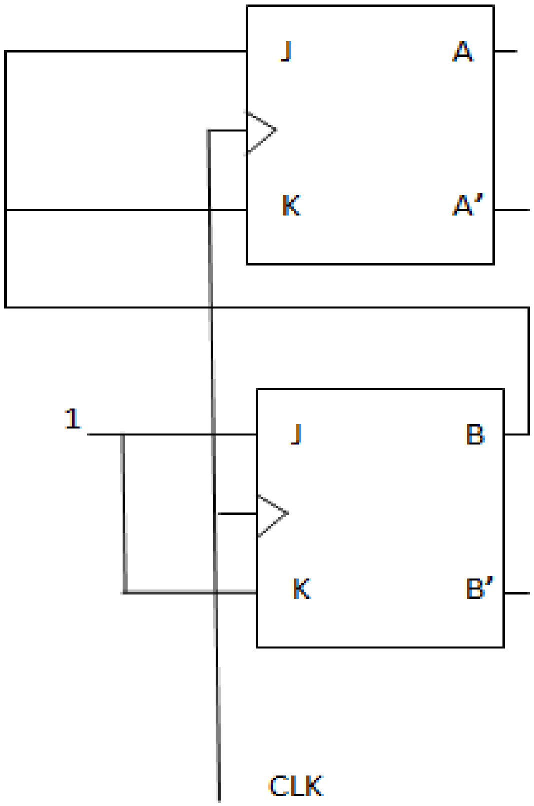
Q(n)	Q(n + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Flip-Flop

A_n	B_n	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

3) $J_A = K_A = B$
$J_B = K_B = 1$

4)



Design a counter that counts the following sequence 1, 6, 7, 3, 2 using T flipflops. Check if it self correcting or not

A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	T_A	T_B	T_C
0	0	0	x	x	x			
0	0	1	1	1	0			
0	1	0	0	0	1			
0	1	1	0	1	0			
1	0	0	x	x	x			
1	0	1	x	x	x			
1	1	0	1	1	1			
1	1	1	0	1	1			

Design a counter that counts the following sequence 1, 6, 7, 3, 2 using T flipflops. Check if it self correcting or not

T Flip-Flop

T	$Q(n+1)$
0	$Q(n)$
1	$Q'(n)$

A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	T_A	T_B	T_C
0	0	0	x	x	x	x		
0	0	1	1	1	0	1		
0	1	0	0	0	1	0		
0	1	1	0	1	0	0		
1	0	0	x	x	x	x		
1	0	1	x	x	x	x		
1	1	0	1	1	1	0		
1	1	1	0	1	1	1		

Design a counter that counts the following sequence 1, 6, 7, 3, 2 using T flipflops. Check if it self correcting or not

T Flip-Flop

T	Q(n + 1)
0	Q(n)
1	Q′(n)

A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	T_A	T_B	T_C
0	0	0	x	x	x	x	x	
0	0	1	1	1	0	1	1	
0	1	0	0	0	1	0	1	
0	1	1	0	1	0	0	0	
1	0	0	x	x	x	x	x	
1	0	1	x	x	x	x	x	
1	1	0	1	1	1	0	0	
1	1	1	0	1	1	1	0	

Design a counter that counts the following sequence 1, 6, 7, 3, 2 using T flipflops. Check if it self correcting or not

***T* Flip-Flop**

T	Q(n + 1)
0	$Q(n)$
1	$Q'(n)$

A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	T_A	T_B	T_C
0	0	0	x	x	x	x	x	x
0	0	1	1	1	0	1	1	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	0

TA

				Bn
	0 X	1 1	3	2
An	4 X	5 X	7 1	6
		Cn		

$$TA = Bn' + An\,Cn$$

TB

				Bn
	0 X	1 1	3	2 1
An	4 X	5 X	7	6
		Cn		

$$TB = Bn' + An'\,Cn'$$

Tc				Bn
	0 X	1 1	3 1	2 1
An	4 X	5 X	7	6 1
			Cn	

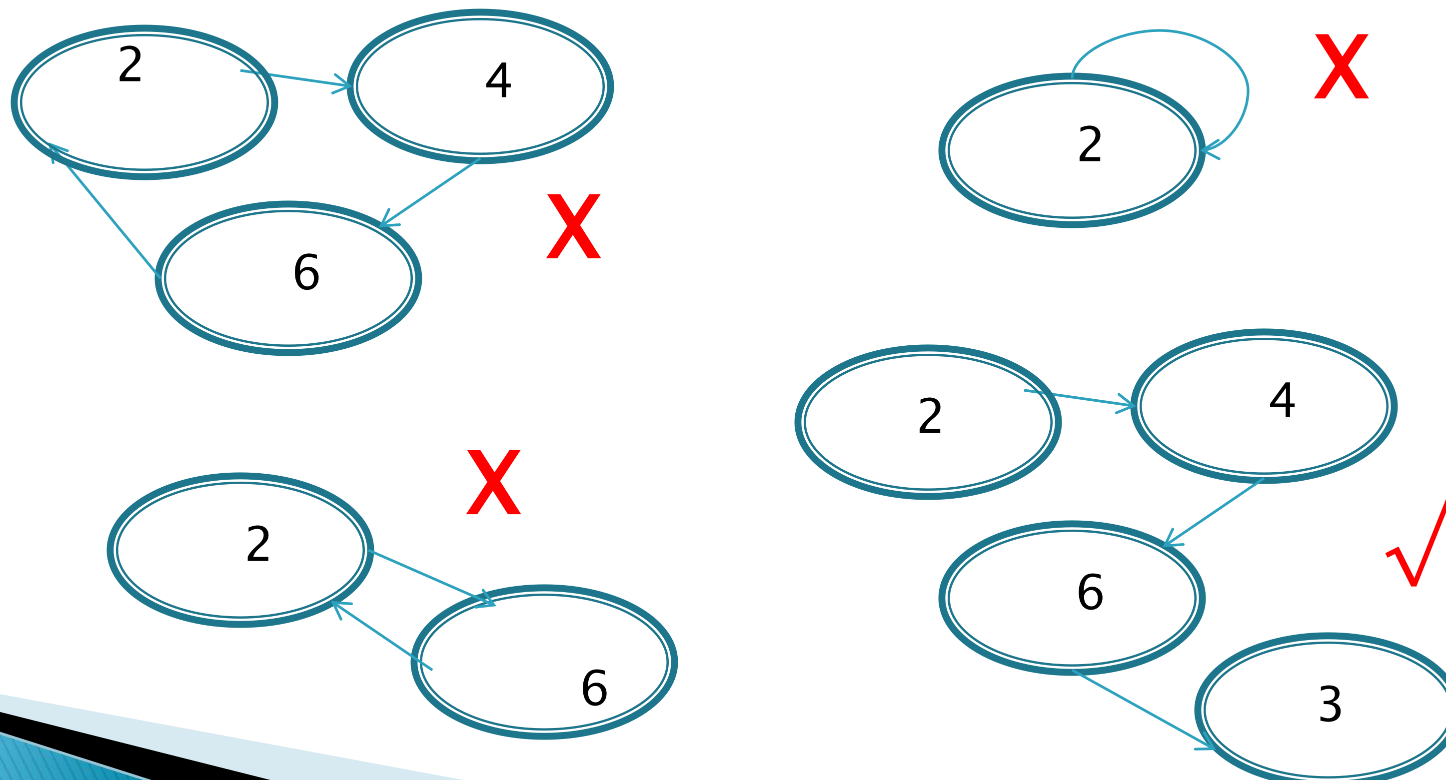
$$TC = An' + Cn' = (An\ Cn)'$$

4) Draw logic diagram

The unused states of this counter are 0
, 4 and 5
Is it self-correcting ??

Examples for self-correcting

- If the unused states are 2, 4 and 6 for example. Let us consider some cases for checking the designed counter



Now what about our counter

$TA = Bn' + An\ Cn$

$TB = Bn' + An'\ Cn'$

$TC = An' + Cn' = (An\ Cn)'$

Unused states

Unused state A B C	Ta Tb Tc	Its next state A B C
0 0 0	1 1 1	1 1 1 √
1 0 0		
1 0 1		

Now what about our counter

TA = Bn' + An Cn

TB = Bn' + An' Cn'

TC = An' + Cn' = (An Cn)'

Unused states

Unused state A B C	Ta Tb Tc	Its next state A B C
0 0 0	1 1 1	1 1 1 √
1 0 0	1 1 1	0 1 1 √
1 0 1		

Now what about our counter

TA = Bn’ + An Cn

TB = Bn’ + An’ Cn’

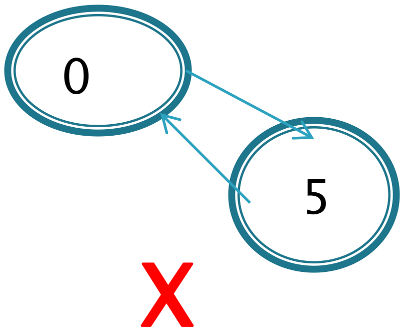
TC = An’ + Cn’ = (An Cn)’

Unused states

Unused state A B C	Ta Tb Tc	Its next state A B C
0 0 0	1 1 1	1 1 1 √
1 0 0	1 1 1	0 1 1 √
1 0 1	1 1 0	0 1 1 √

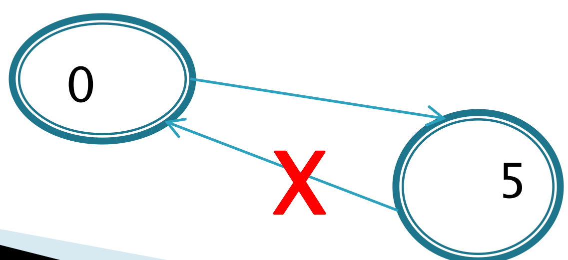
Counter is self correcting

What if



A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	T_A	T_B	T_C
0	0	0	X	X	X	X	X	X
0	0	1	1	1	0	1	1	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	X	X	X	X	X	X
1	0	1	0 X	1 X	0 X	1 X	1 X	1 X
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	0

What we can do ??



Break the loop, update the table and redesign (repeat the maps)

Next Lecture we will explain analysis of sequential circuits
thank you