# Digital Design

Lecture of week 8

Dr Manal Tantawi

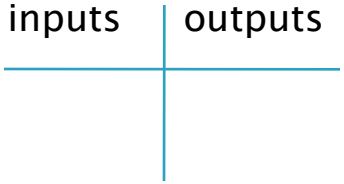
# Chapter 5
# Sequential Circuits

# Synchronous Sequential Circuits

Combinational circuits Vs Sequential Circuits

## Combinational Circuits

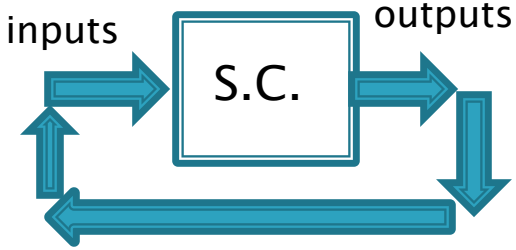
- Gates
- No feedback

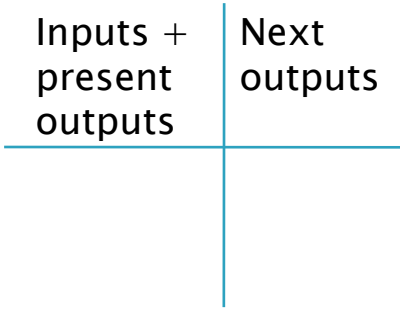




- Time independent

## Sequential Circuits

- Gates + memory units
- Feedback

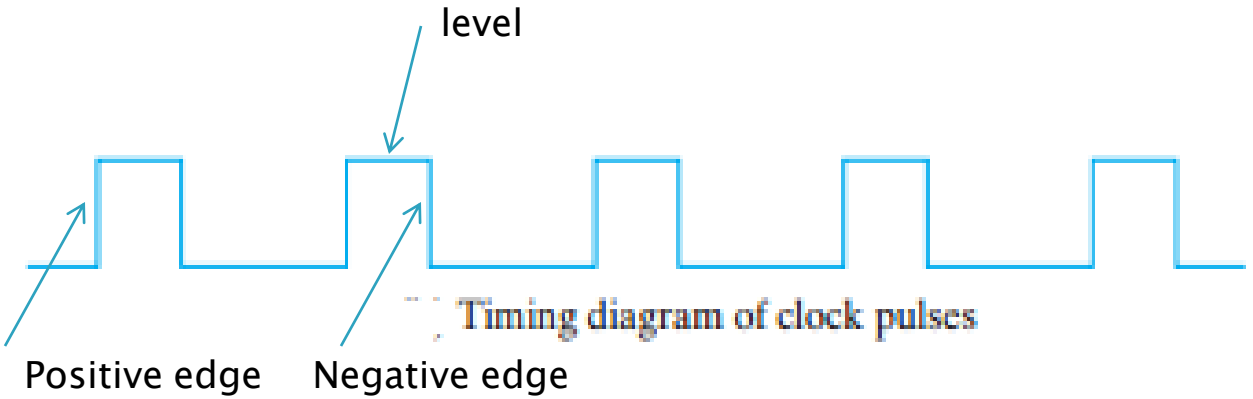



- Time dependent

(Clock )

# Clock




Level Trigger

Latches

(a) Response to positive level

Positive Edge Trigger

(b) Positive-edge response

Negative Edge Trigger

(c) Negative-edge response

Flip flops

# Clock continued..

Cycle period T

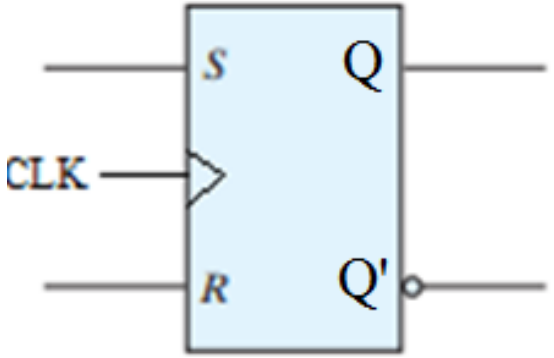
T = 1/Frequency (F)

For example T = 0.5 sec F = 2 HZ
T= 0.25 sec F =4 HZ

# Latches & Flip Flops

- RS Flipflop

| R | S | Qn | Qn+1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | undeterm |
| 1 | 1 | 1 | |



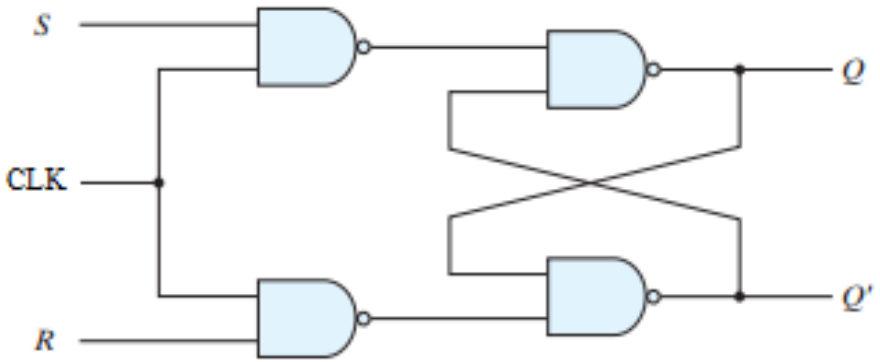

Characteristic table

| R | S | Qn+1 | |
|---|---|---|---|
| 0 | 0 | No change | Qn |
| 0 | 1 | set | 1 |
| 1 | 0 | reset | 0 |
| 1 | 1 | Indeterminate | |

# Latches & Flip Flops

- RS Latch

| R | S | Qn | Qn+1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | undeterm |
| 1 | 1 | 1 | |



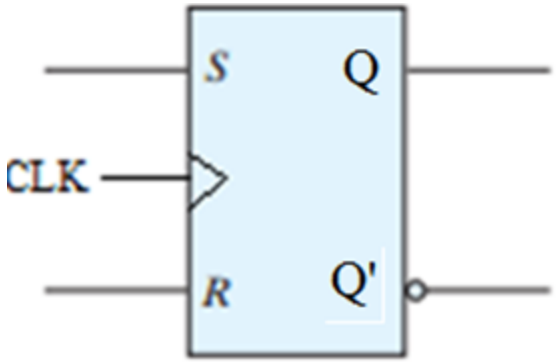

Characteristic table

| CLK | R | S | Qn+1 |
|---|---|---|---|
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | set |
| 1 | 1 | 0 | reset |
| 1 | 1 | 1 | Indeterminate |

# Latches & Flip Flops

- RS Flip Flop

| R | S | Qn | Qn+1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | undeterm |
| 1 | 1 | 1 | |



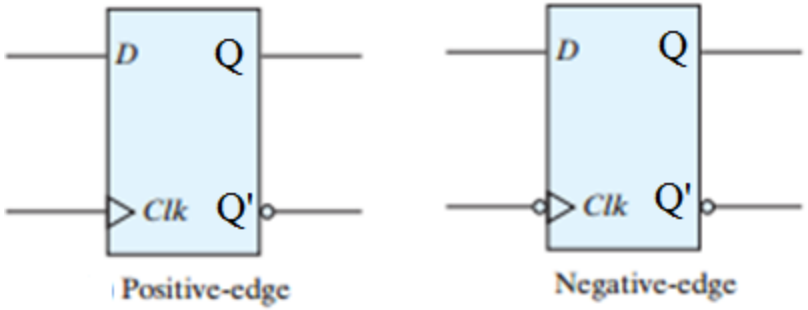

Characteristic table

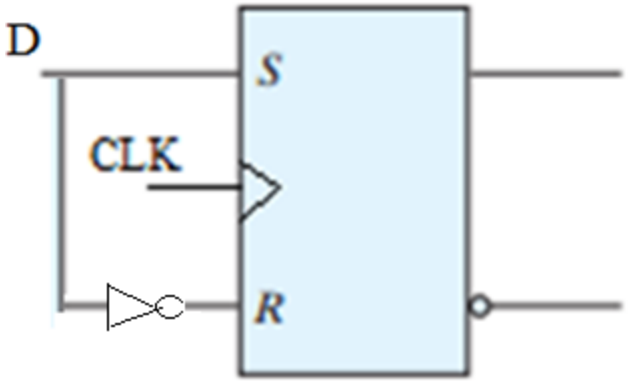
| R | S | Qn+1 | |
|---|---|---|---|
| 0 | 0 | No change | Qn |
| 0 | 1 | set | 1 |
| 1 | 0 | reset | 0 |
| 1 | 1 | Indeterminate | |

# Flip flops

- D Flip Flop

| D | Qn | Qn+1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |




Characteristic table

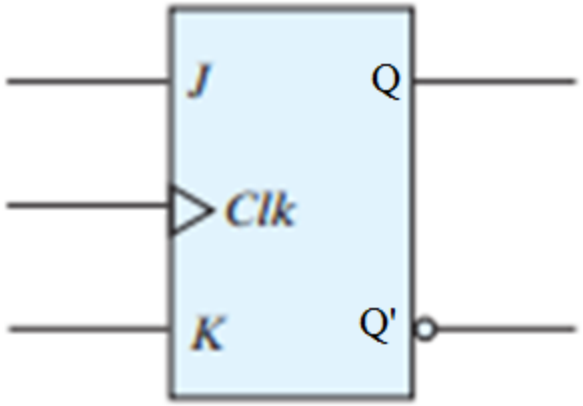
**D Flip-Flop**

| D | Q(n + 1) | |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |

# Flip Flops

- JK Flip Flop

| J | K | Qn | Qn+1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




Characteristic table

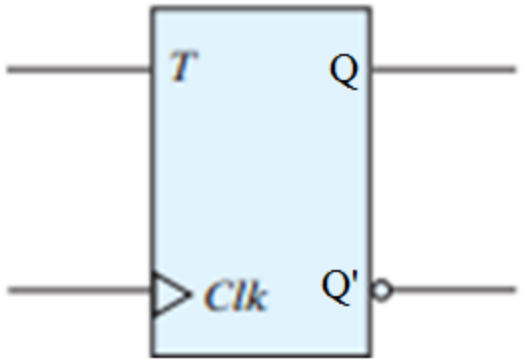
**JK Flip-Flop**

| J | K | Q(n + 1) | |
|---|---|---|---|
| 0 | 0 | $Q(n)$ | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | $Q'(n)$ | Complement |

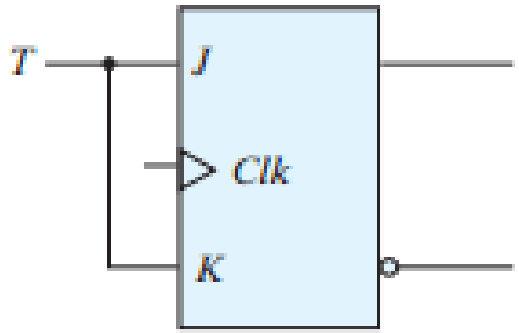
# Flip flops

- T Flip Flop

| T | Qn | Qn+1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



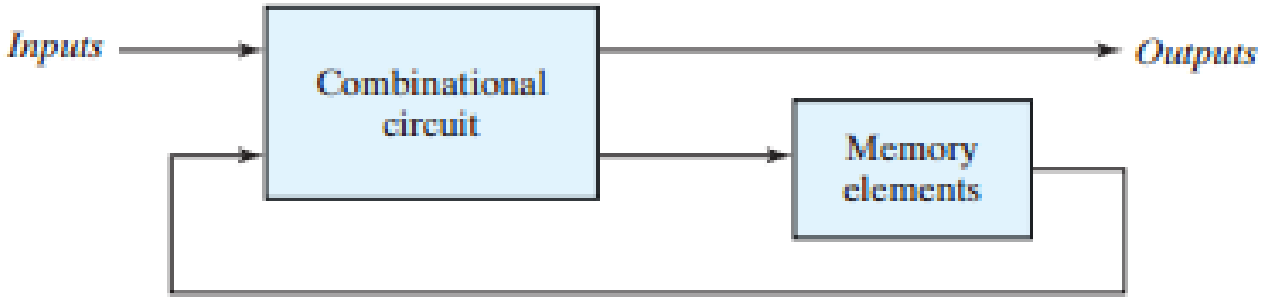

Characteristic table



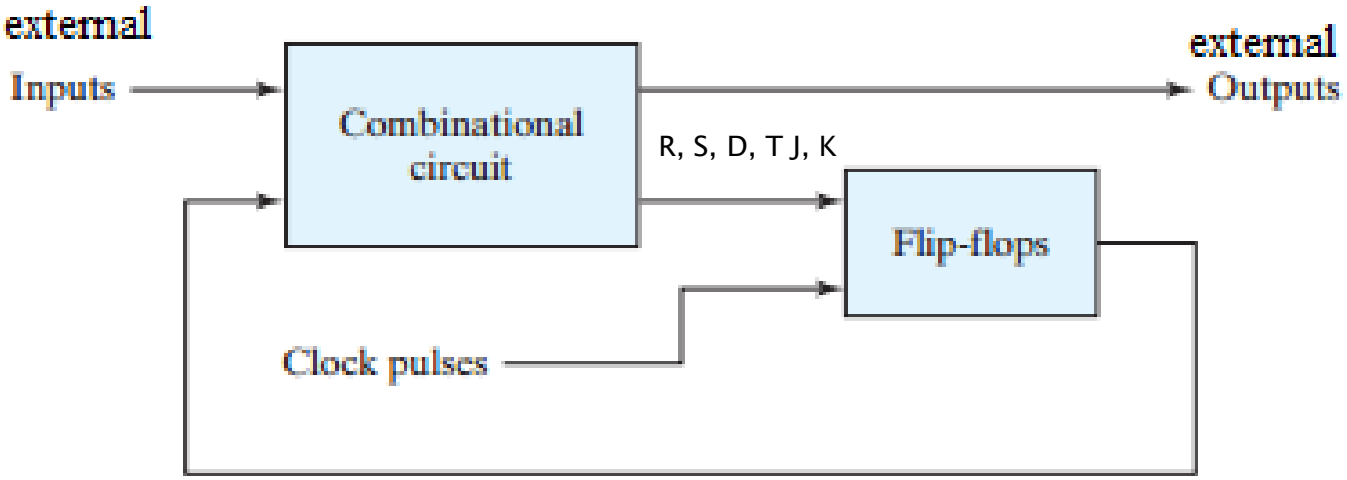

**T Flip-Flop**

| T | Q(n + 1) | |
|---|---|---|
| 0 | $Q(n)$ | No change |
| 1 | $Q'(n)$ | Complement |

# Synchronous Sequential Circuits



# Synchronous Sequential Circuits



# Synchronous Sequential Circuits

Design Procedure

1) State Diagram

2) Number of ex. Inputs and outputs and number of flipflops

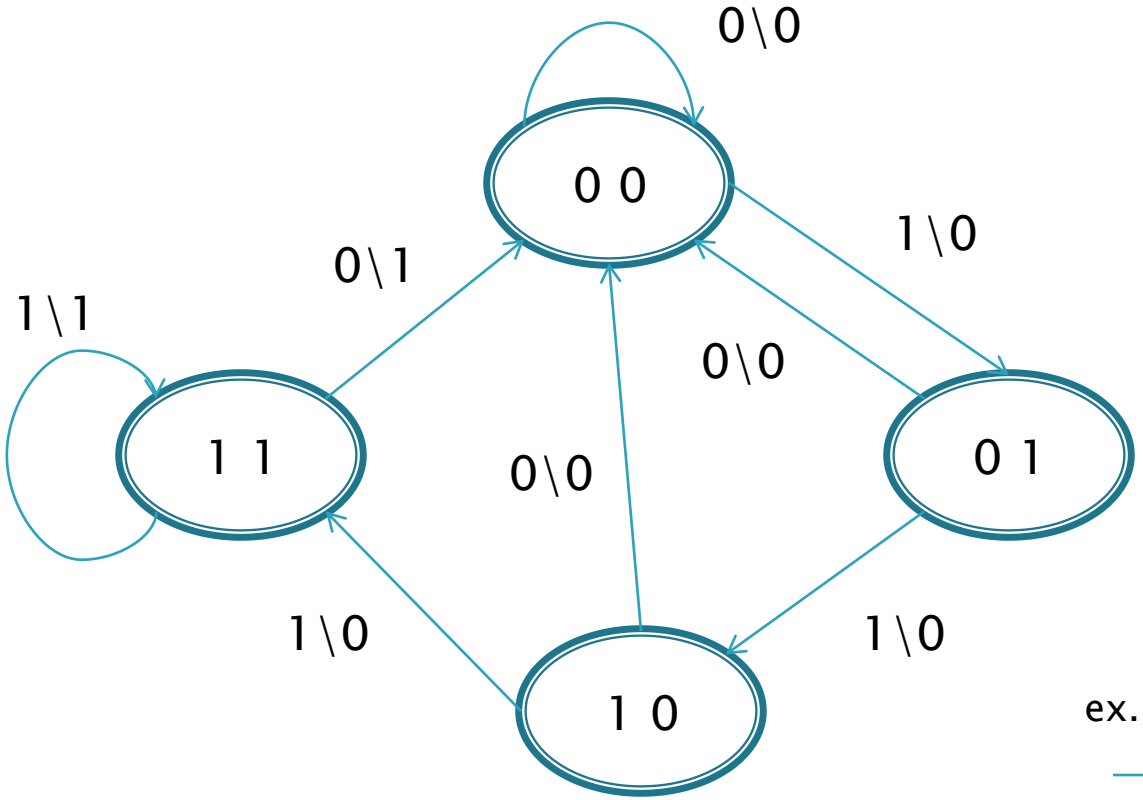
3) State Table

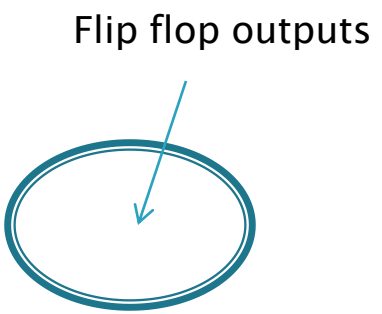
4) Simplified expressions using Kmap for external outputs and inputs of flipflops

5) Logic diagram

# Synchronous Sequential Circuits

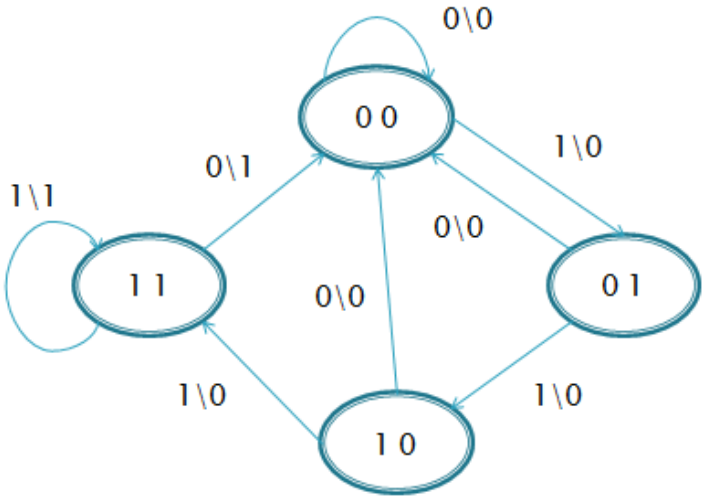
Design a sequential circuit that follows the following state diagram using D flip flops




2) Two flip flops , one ex. Input & one ex. output

3) state table



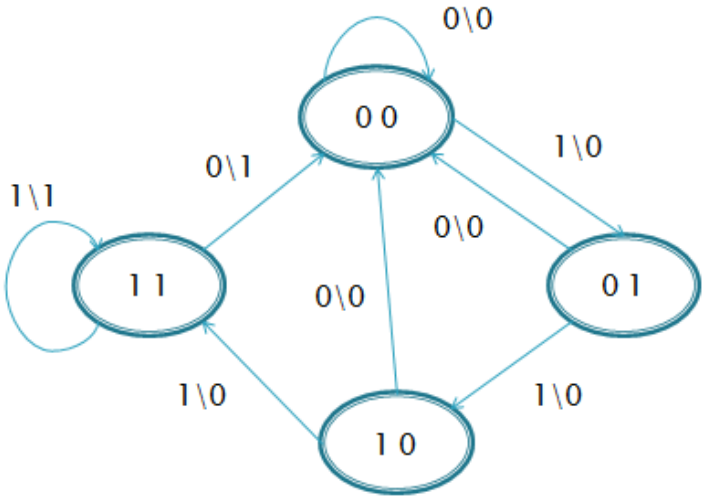

Present outputs next outputs

| An | Bn | X | An+1 | Bn+1 | $D_A$ | $D_B$ | Y |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | | | 0 |
| 0 | 0 | 1 | 0 | 1 | | | 0 |
| 0 | 1 | 0 | 0 | 0 | | | 0 |
| 0 | 1 | 1 | 1 | 0 | | | 0 |
| 1 | 0 | 0 | 0 | 0 | | | 0 |
| 1 | 0 | 1 | 1 | 1 | | | 0 |
| 1 | 1 | 0 | 0 | 0 | | | 1 |
| 1 | 1 | 1 | 1 | 1 | | | 1 |

3) state table

**D Flip-Flop**

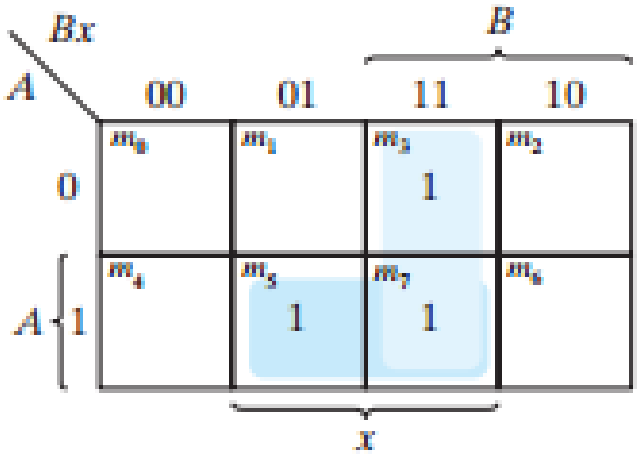
| D | Q(n + 1) | |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |



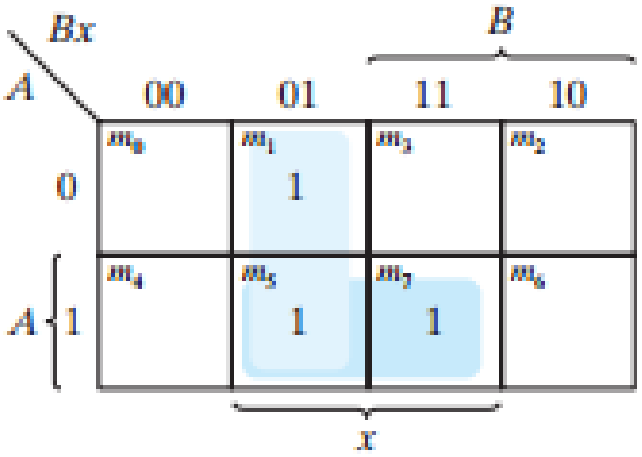

Present outputs next outputs

| An | Bn | X | An+1 | Bn+1 | $D_A$ | $D_B$ | Y |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

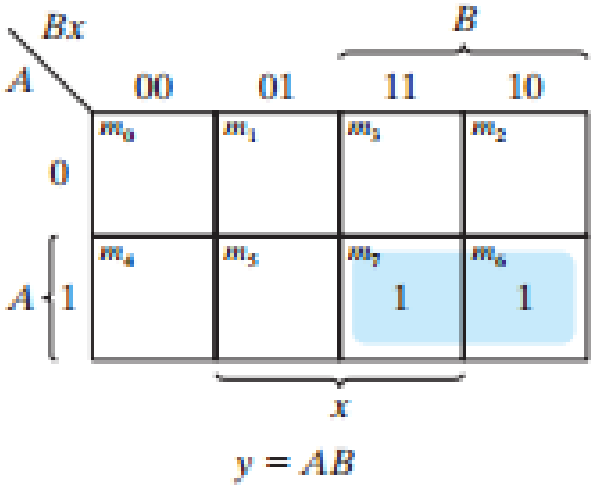
4) Kmaps for ex. Output and flip flops inputs




$D_A = Ax + Bx$

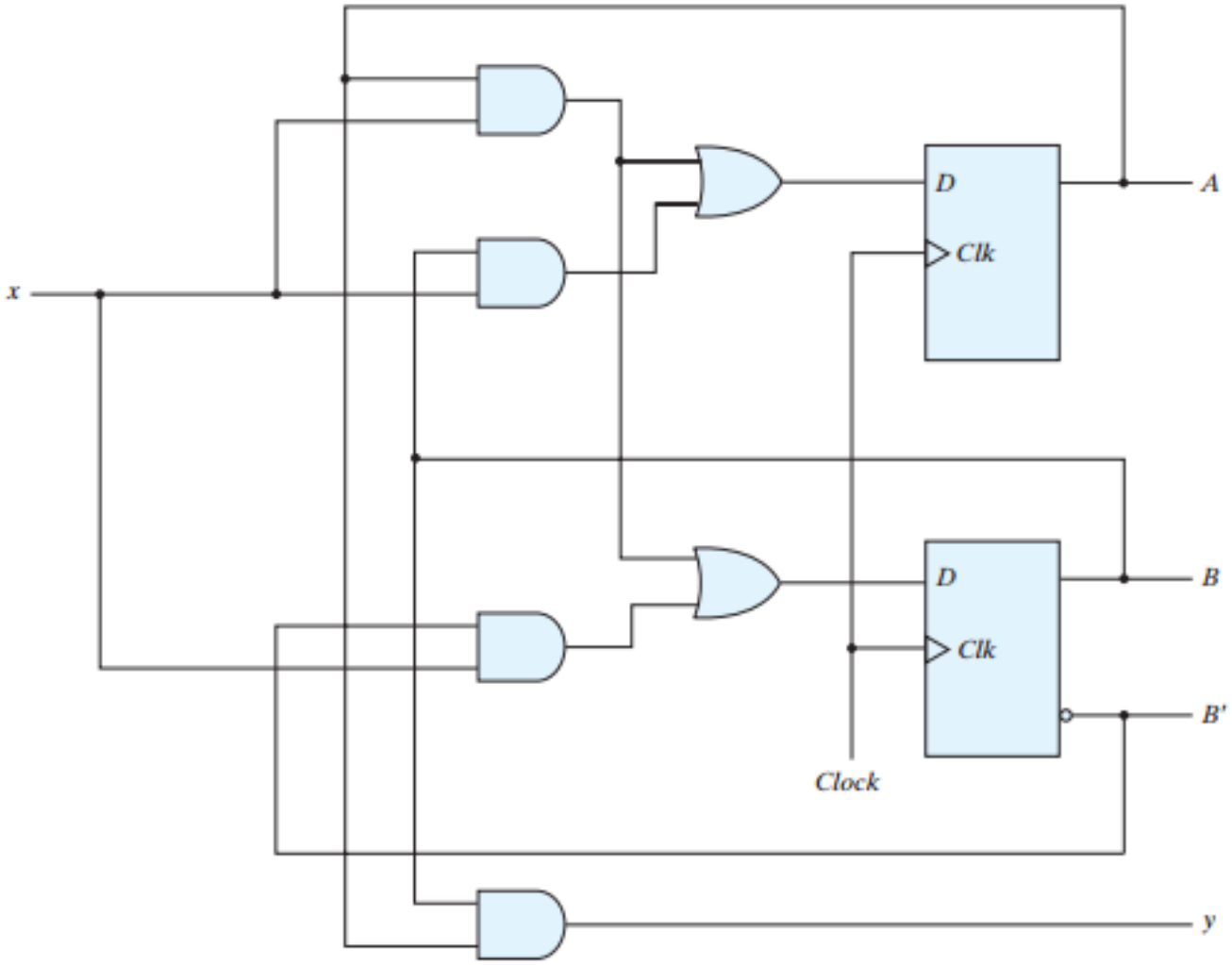



$D_B = Ax + B'x$

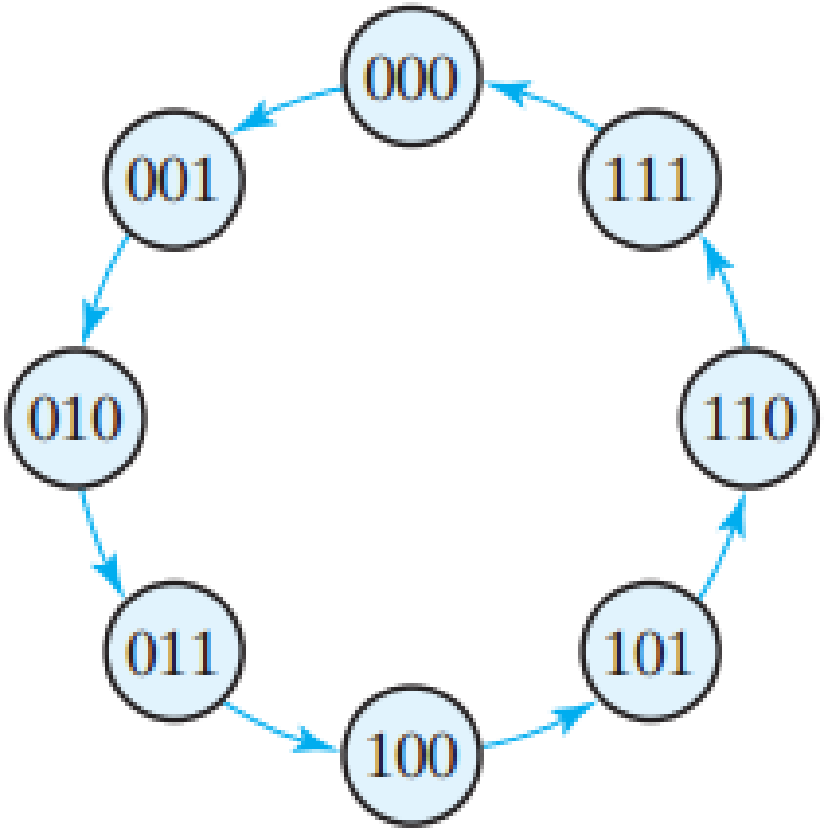



$y = AB$

- Logic diagram



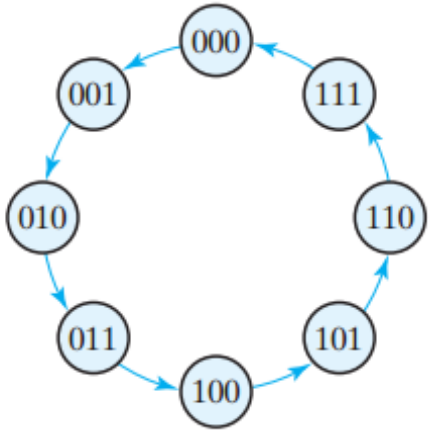
Design a sequential circuit that follows the following state diagram using T flip flops




2) 3 flip flops , no ex. Input & no ex. output

**T Flip-Flop**

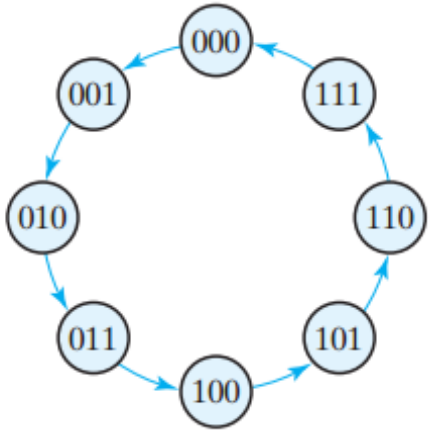
| T | Q(n + 1) | |
|---|---|---|
| 0 | $Q(n)$ | No change |
| 1 | $Q'(n)$ | Complement |




| A2n | A1n | A0n | A2n+1 | A1n+1 | A0n+1 | Ta2 | Ta1 | Ta0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | | |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | | |

**T Flip-Flop**

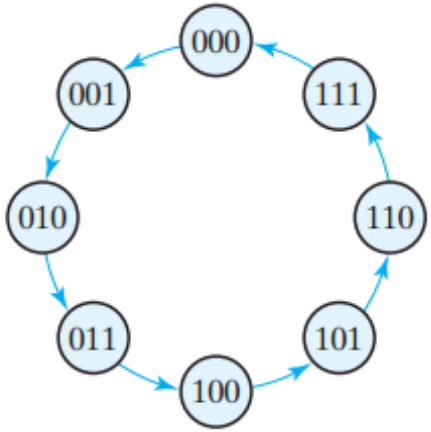
| T | Q(n + 1) | |
|---|---|---|
| 0 | $Q(n)$ | No change |
| 1 | $Q'(n)$ | Complement |




| A2n | A1n | A0n | A2n+1 | A1n+1 | A0n+1 | Ta2 | Ta1 | Ta0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | |

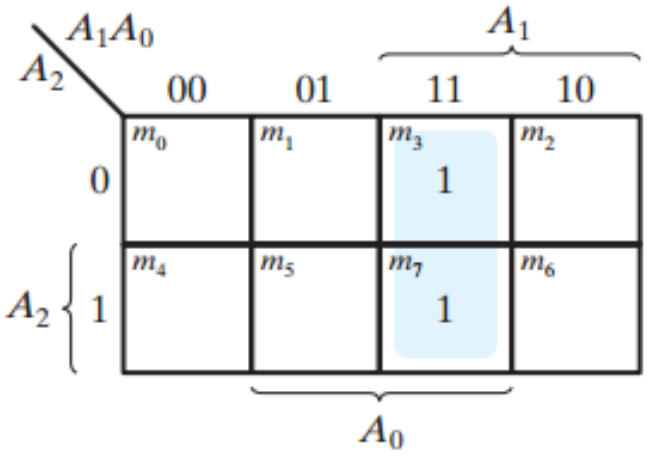
**T Flip-Flop**

| T | Q(n + 1) | |
|---|---|---|
| 0 | $Q(n)$ | No change |
| 1 | $Q'(n)$ | Complement |

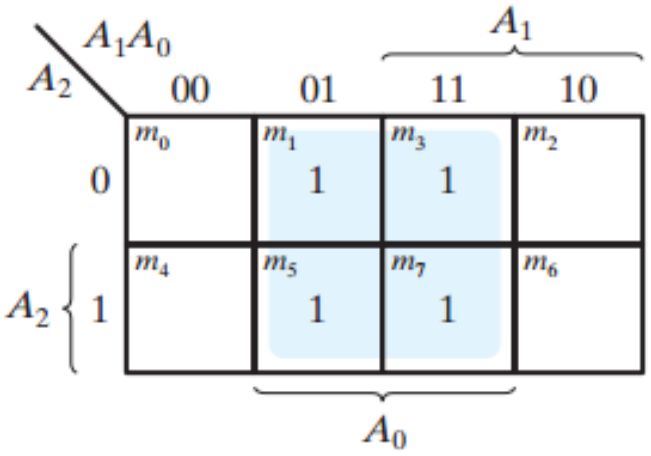



| A2n | A1n | A0n | A2n+1 | A1n+1 | A0n+1 | Ta2 | Ta1 | Ta0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

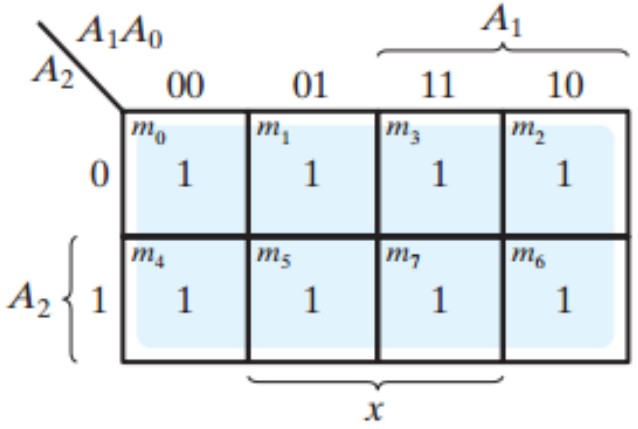
4) Kmaps for flip flops inputs




$T_{A2} = A_1A_0$

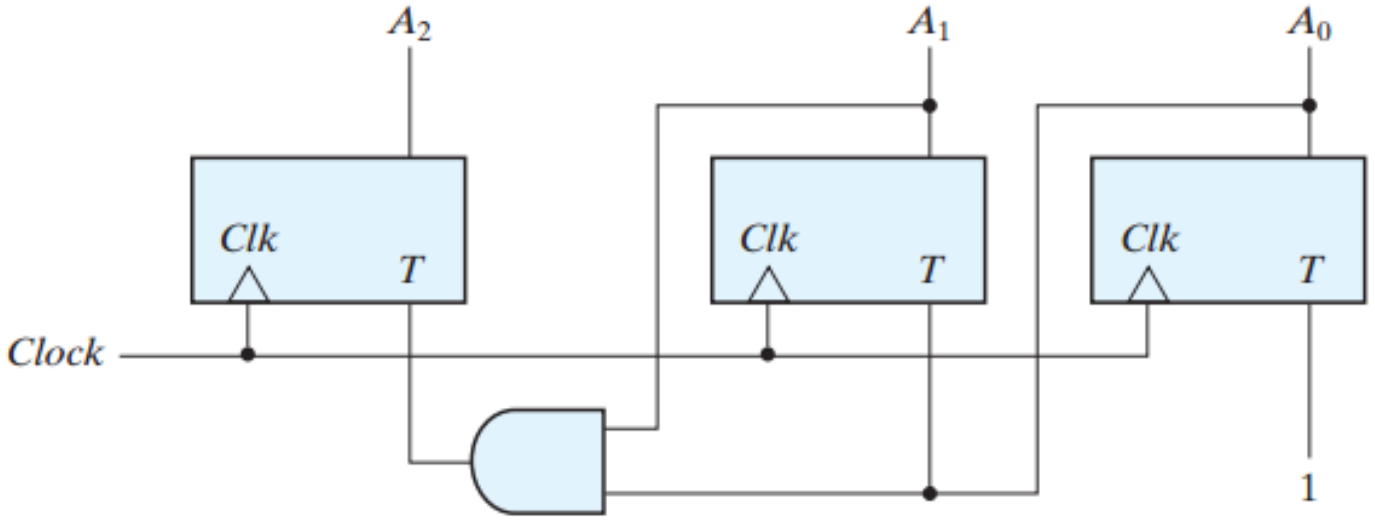



$T_{A1} = A_0$




$T_{A0} = 1$

- Logic diagram



Next Lecture we will continue chapter 5 thank you