Digital Design

Lecture of week 11

Dr Manal Tantawi

Analysis of Sequential Circuits

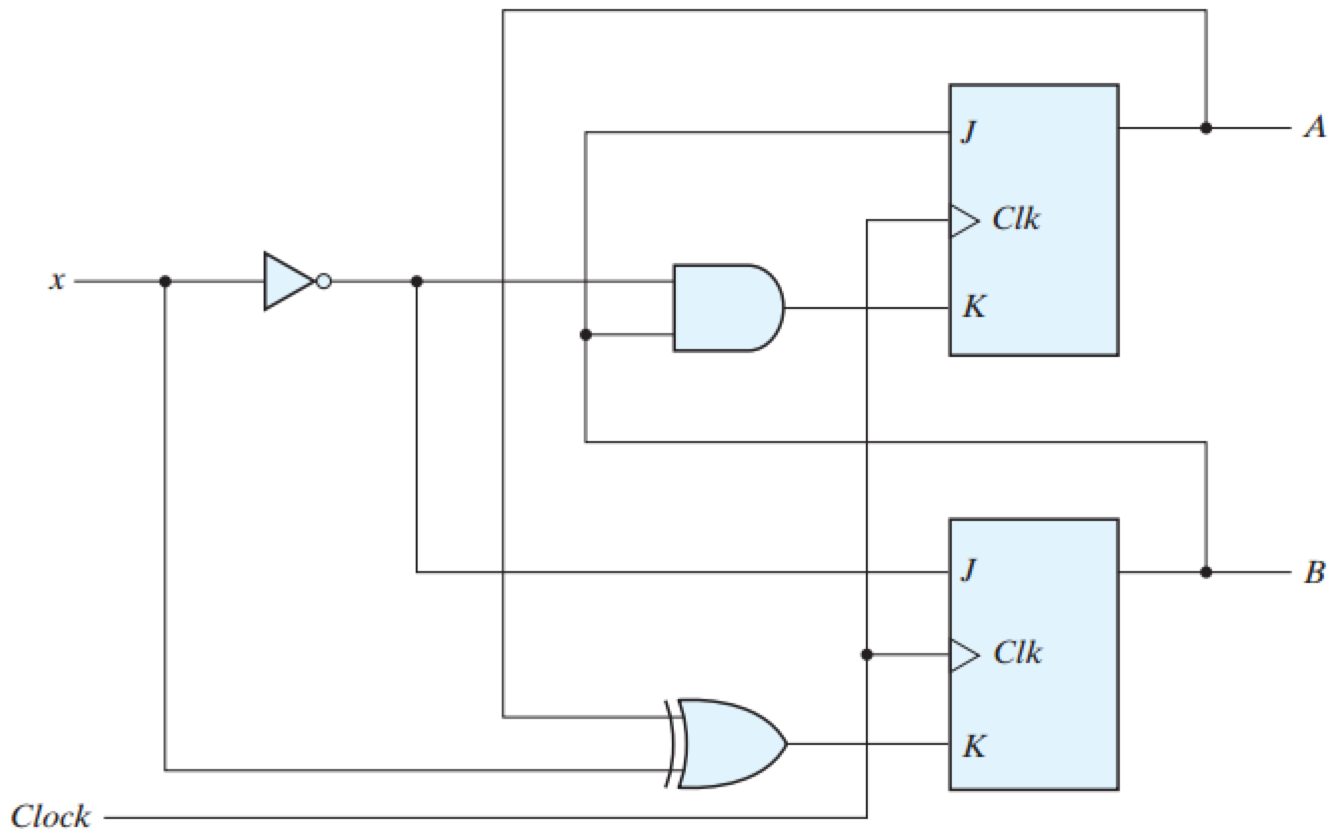
1) Logic Diagram

2) Expressions for external outputs (if exist) and inputs of flipflops

3) State Table

4) State Diagram

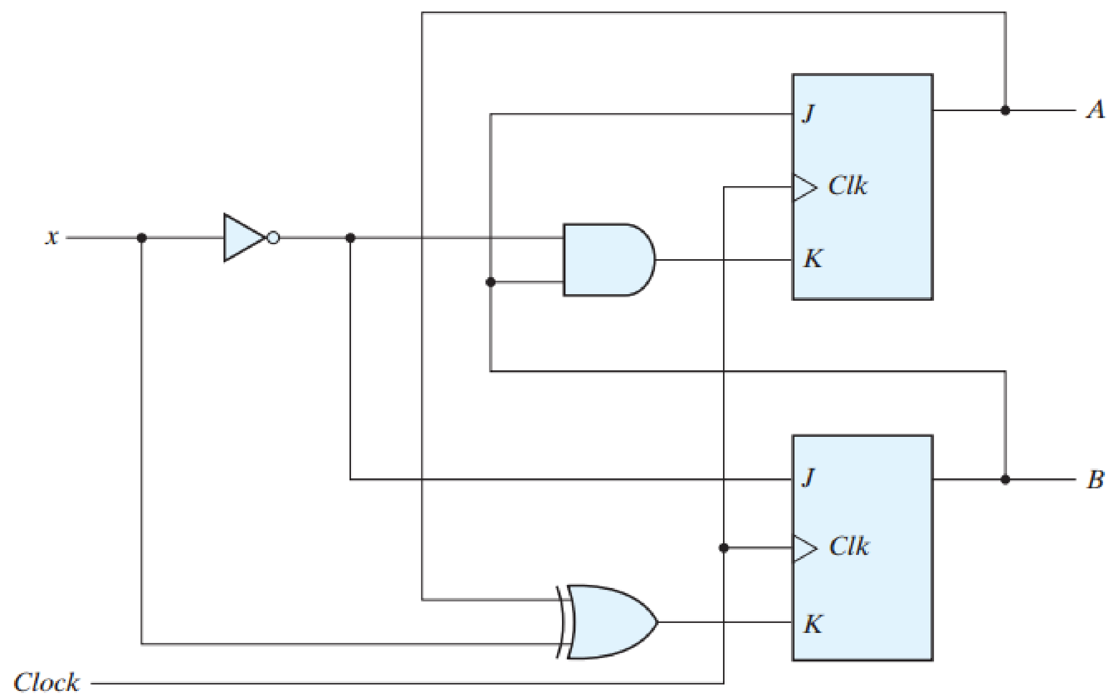
Analyze the following circuit and then derive its state table and diagram



- One external input
- No external output
- Two J K flip flops

$$J_A = B \quad K_A = Bx'$$

$$J_B = x' \quad K_B = A'x + Ax' = A \oplus x$$



$$J_A = B \quad K_A = Bx'$$

$$J_B = x' \quad K_B = A'x + Ax' = A \oplus x$$

State Table for Sequential Circuit with JK Flip-Flops

Present State		Input	Flip-Flop Inputs				Next State	
A	**B**	**x**	J_A	K_A	J_B	K_B	**A**	**B**
0	0	0	0	0	1	0		
0	0	1	0	0	0	1		
0	1	0	1	1	1	0		
0	1	1	1	0	0	1		
1	0	0	0	0	1	1		
1	0	1	0	0	0	0		
1	1	0	1	1	1	1		
1	1	1	1	0	0	0		

JK Flip-Flop

J	K	Q(n + 1)	
0	0	Q(n)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q′(n)	Complement

State Table for Sequential Circuit with JK Flip-Flops

Present State		Input	Flip-Flop Inputs				Next State	
A	B	x	J_A	K_A	J_B	K_B	A	B
0	0	0	0	0	1	0	0	
0	0	1	0	0	0	1	0	
0	1	0	1	1	1	0	1	
0	1	1	1	0	0	1	1	
1	0	0	0	0	1	1	1	
1	0	1	0	0	0	0	1	
1	1	0	1	1	1	1	0	
1	1	1	1	0	0	0	1	

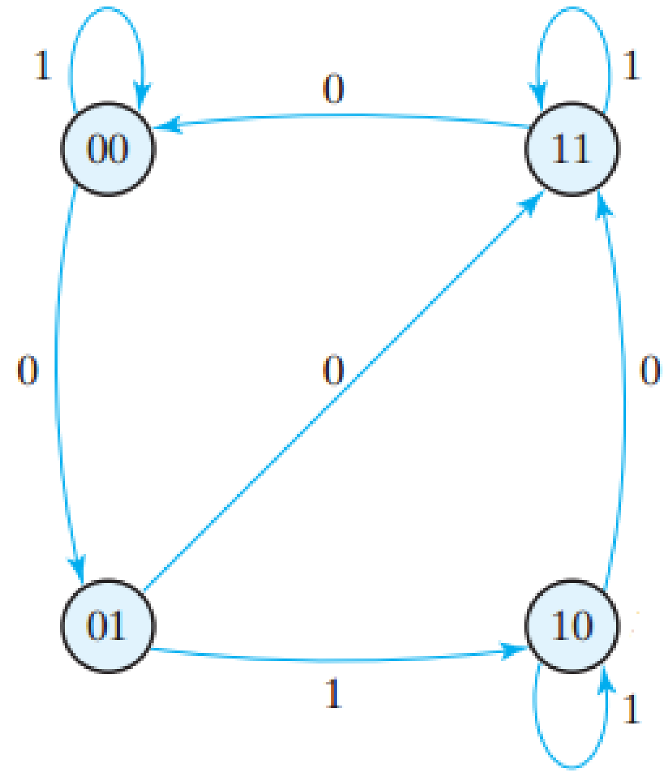
JK Flip-Flop			
J	*K*	Q(n + 1)	
0	0	*Q*(n)	No change
0	1	0	Reset
1	0	1	Set
1	1	*Q'*(n)	Complement

State Table for Sequential Circuit with JK Flip-Flops

Present State		Input	Flip-Flop Inputs				Next State	
A	*B*	*x*	J_A	K_A	J_B	K_B	*A*	*B*
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

Present State		Input	Next State	
A	*B*	*x*	*A*	*B*
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

State Diagram



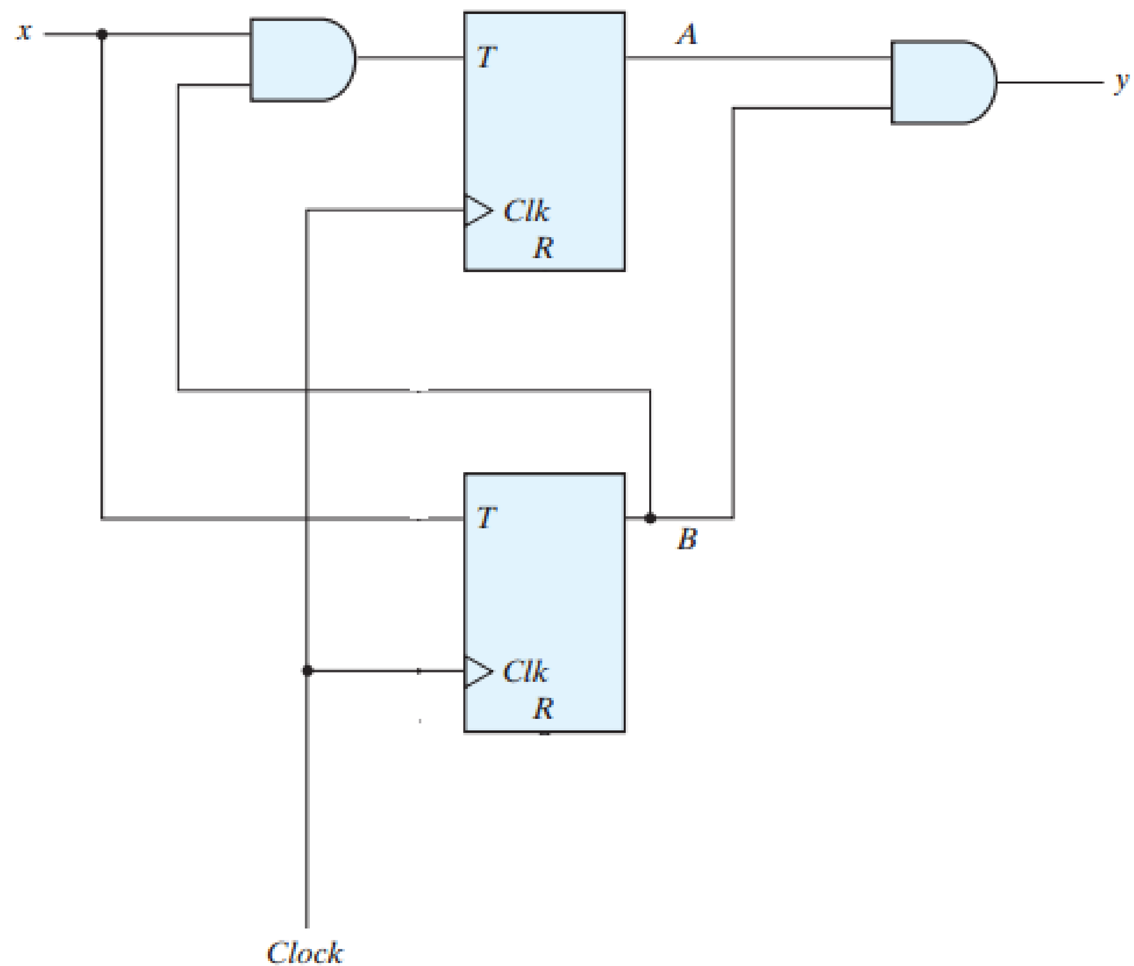
Analyze the following circuit and then derive its state table and diagram

One external input
One external output
Two T flip flops

$$T_A = Bx$$

$$T_B = x$$

$$y = AB$$



$$T_A = Bx$$
$$T_B = x$$
$$y = AB$$

Present State		Input	y
A	B	x	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$T_A = Bx$

$T_B = x$

$y = AB$

Present State		Input			
A	B	x	Ta	Tb	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	1	1	1

$T_A = Bx$

$T_B = x$

$y = AB$

T Flip-Flop

T	Q(n + 1)	
0	$Q(n)$	No change
1	$Q'(n)$	Complement

Present State		Input			Next State	
A	B	x	Ta	Tb	A	y
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	1	0	1	1	0
1	1	0	0	0	1	1
1	1	1	1	1	0	1

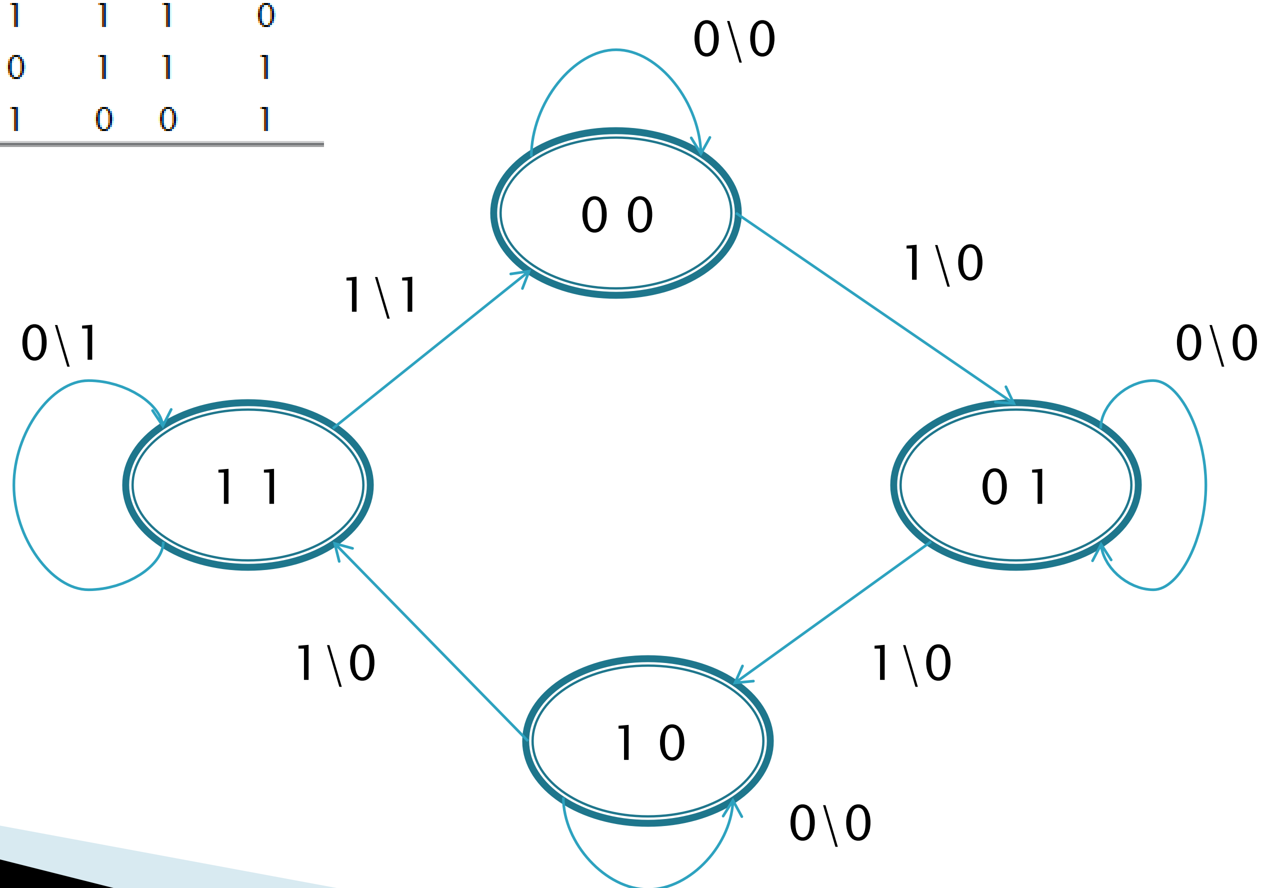
$$T_A = Bx$$
$$T_B = x$$
$$y = AB$$

T Flip-Flop

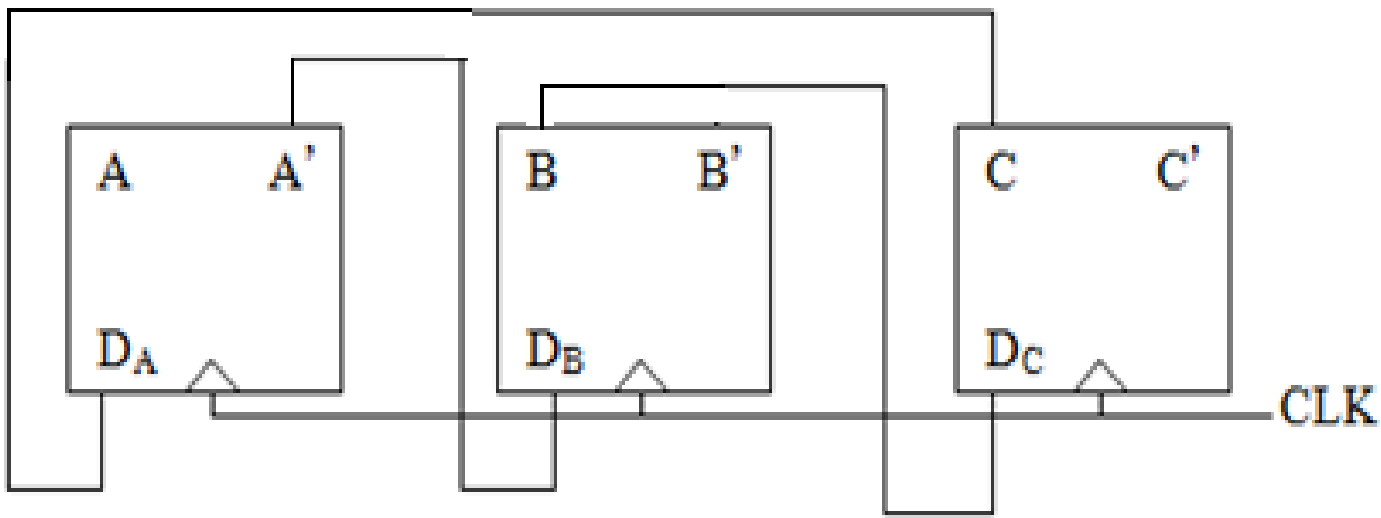
T	Q(n + 1)	
0	$Q(n)$	No change
1	$Q'(n)$	Complement

Present State		Input			Next State		
A	B	x	Ta	Tb	A	B	y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	0	1	0	0
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1

Present State		Input			Next State		
A	*B*	*x*	Ta	Tb	A	B	y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	0	1	0	0
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1



Analyze the following sequential circuit, find state table, state diagram and the repeated sequence if exists. is it self correcting ? why ?



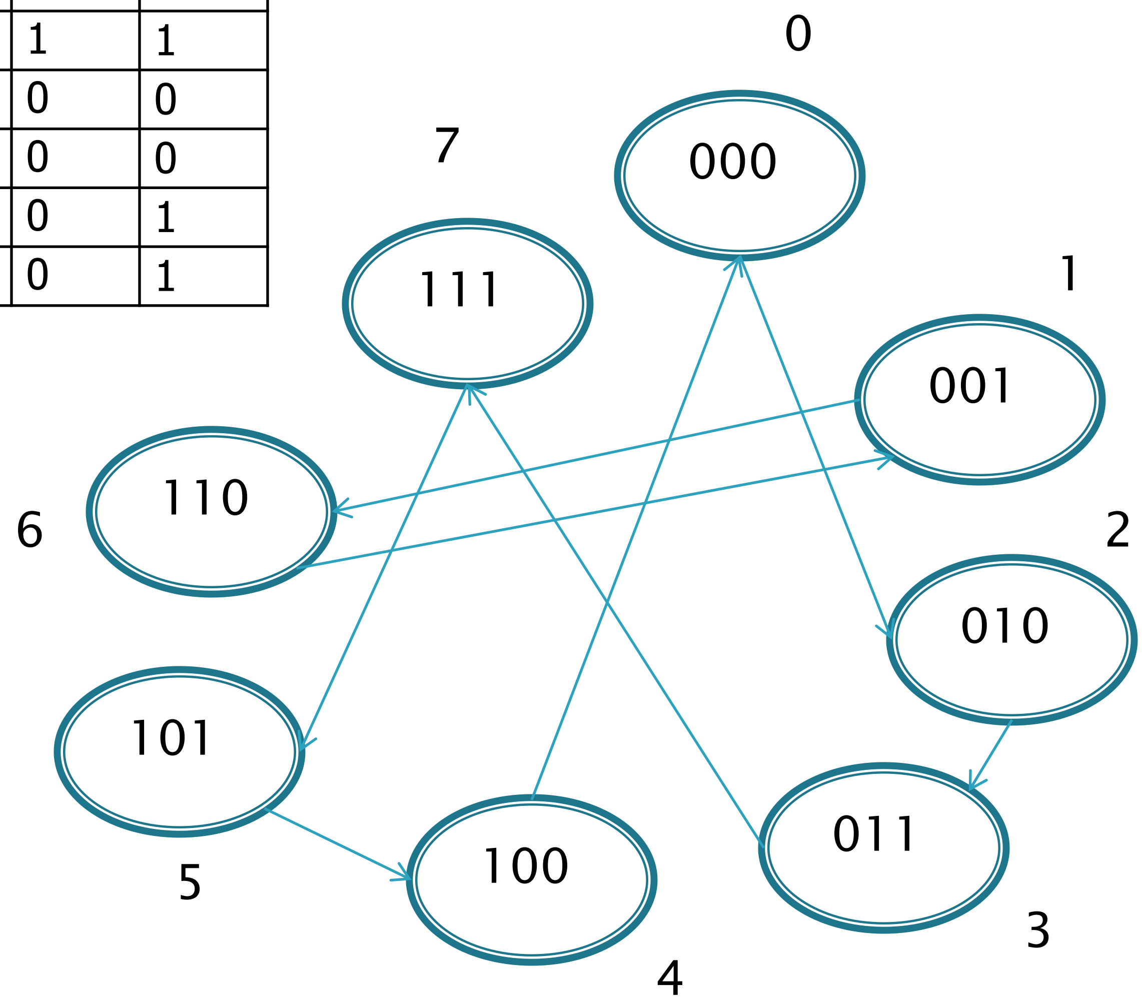
Da = Cn
Db = An’
Dc = Bn

An	Bn	Cn	Da	Db	Dc	An+1	Bn+1	Cn+1
0	0	0	0	1	0			
0	0	1	1	1	0			
0	1	0	0	1	1			
0	1	1	1	1	1			
1	0	0	0	0	0			
1	0	1	1	0	0			
1	1	0	0	0	1			
1	1	1	1	0	1			

Da = Cn
Db = An’
Dc = Bn

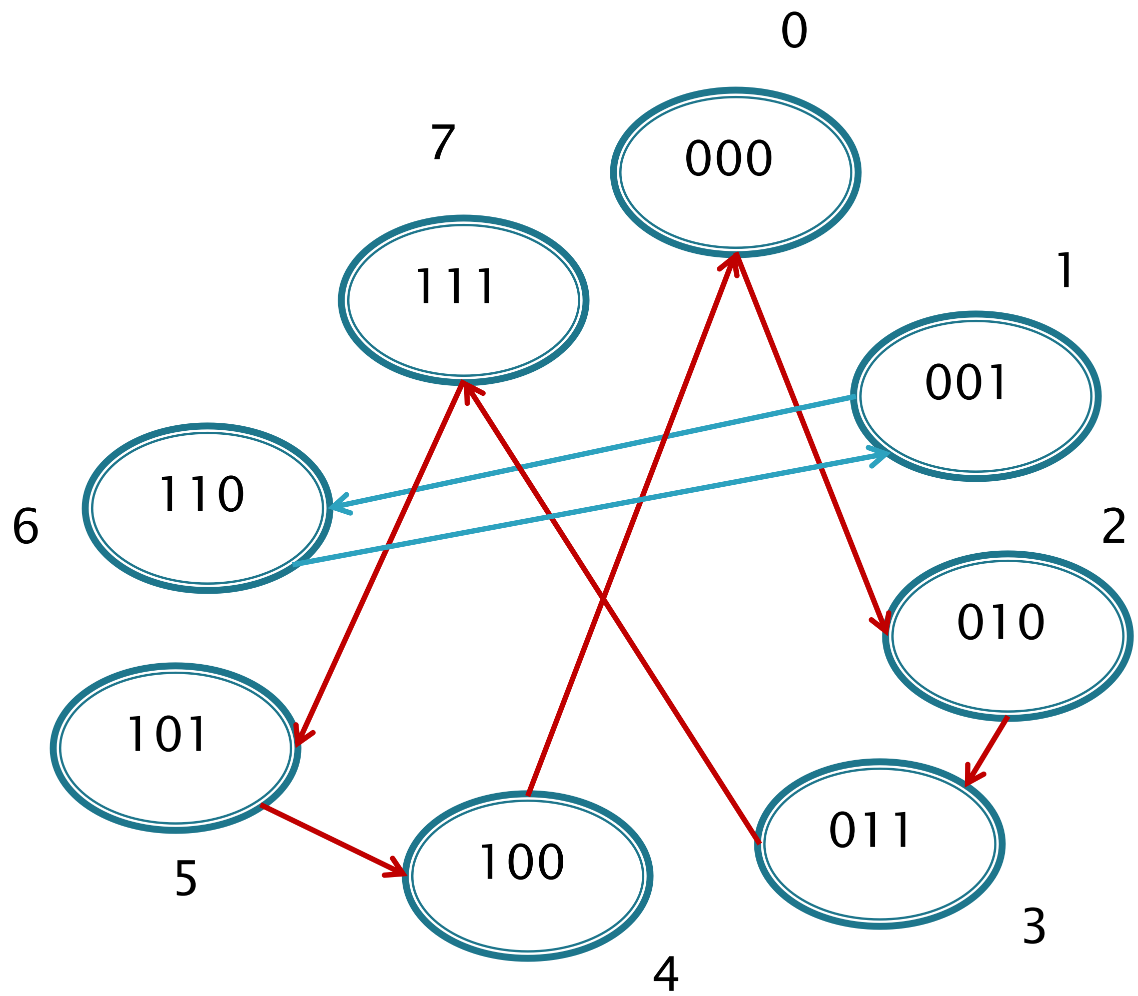
An	Bn	Cn	Da	Db	Dc	An+1	Bn+1	Cn+1
0	0	0	0	1	0	0	1	0
0	0	1	1	1	0	1	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	1	1	0	1	1	0	1

An	Bn	Cn	Da	Db	Dc	An+1	Bn+1	Cn+1
0	0	0	0	1	0	0	1	0
0	0	1	1	1	0	1	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	1	1	0	1	1	0	1



Two existing loops

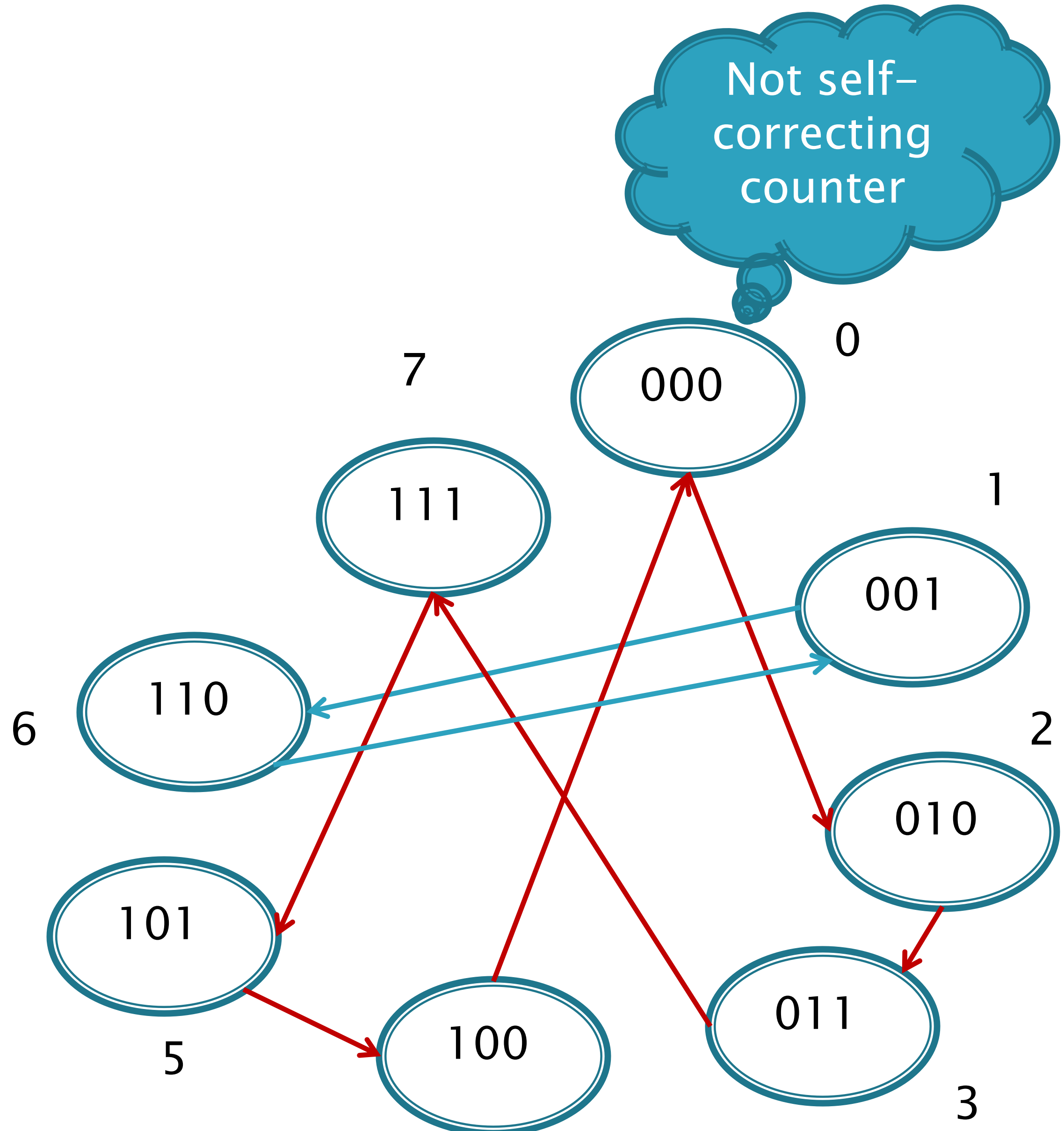
1) 1 and 6
2) 7, 5, 4, 0, 2, 3



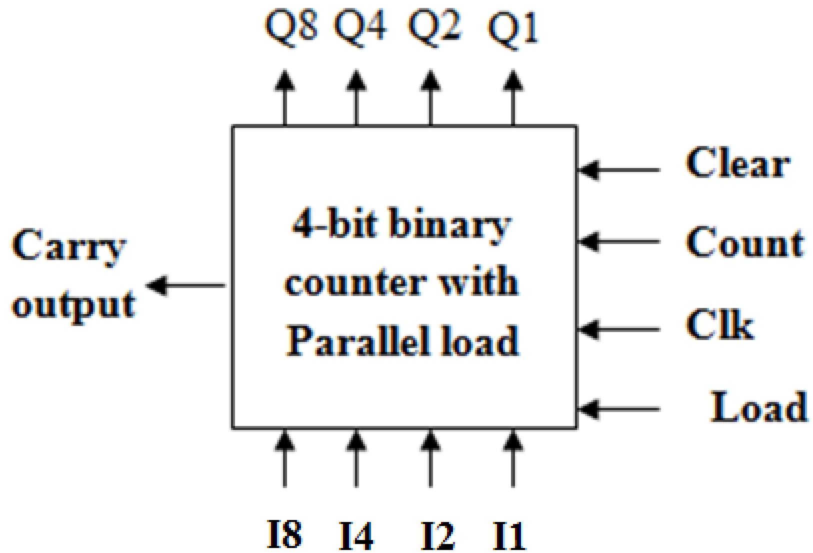
Two existing loops

1) 1 and 6
2) 7, 5, 4, 0, 2, 3

Self correcting counter contains only one loop

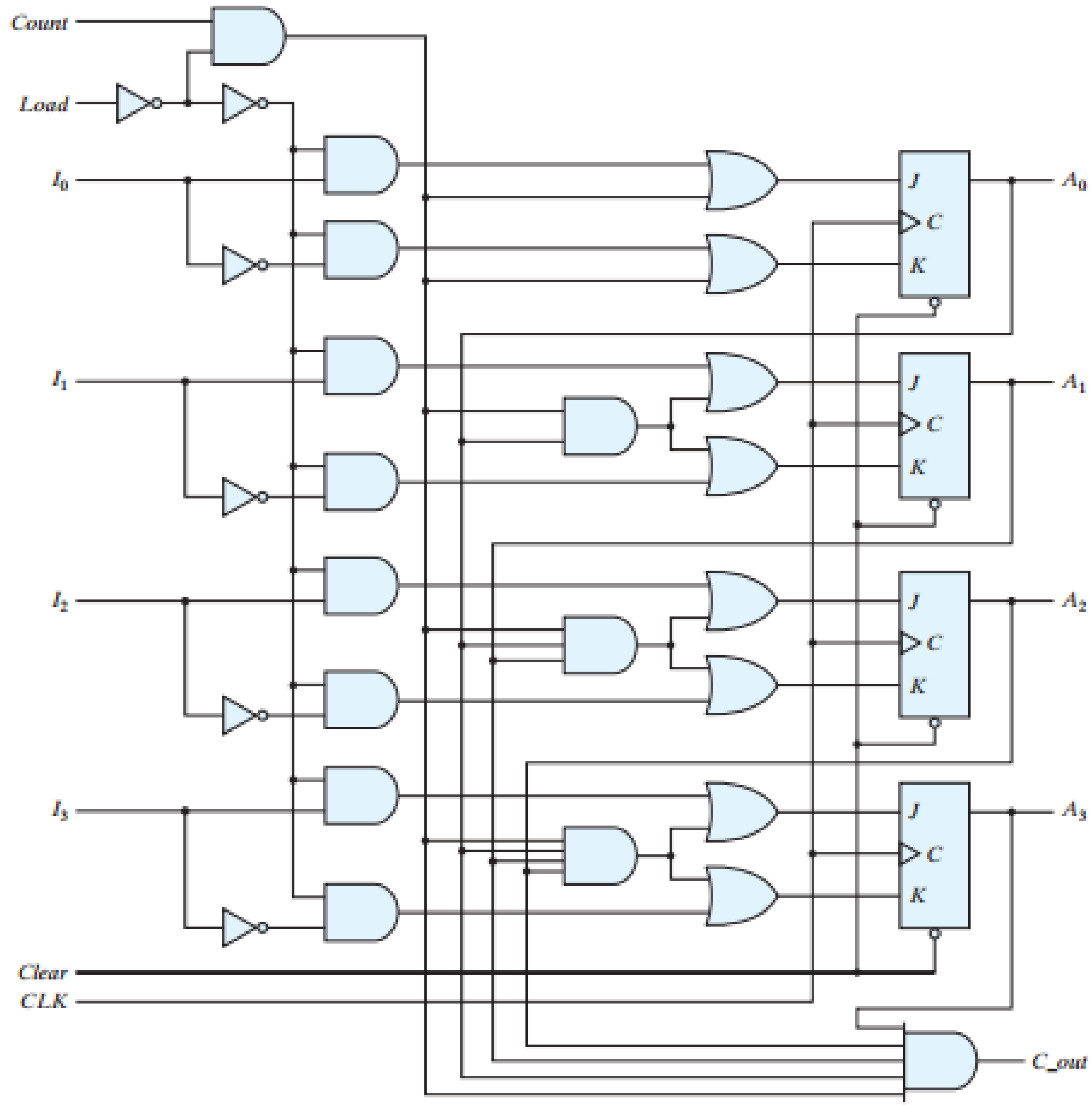


Programmable counters

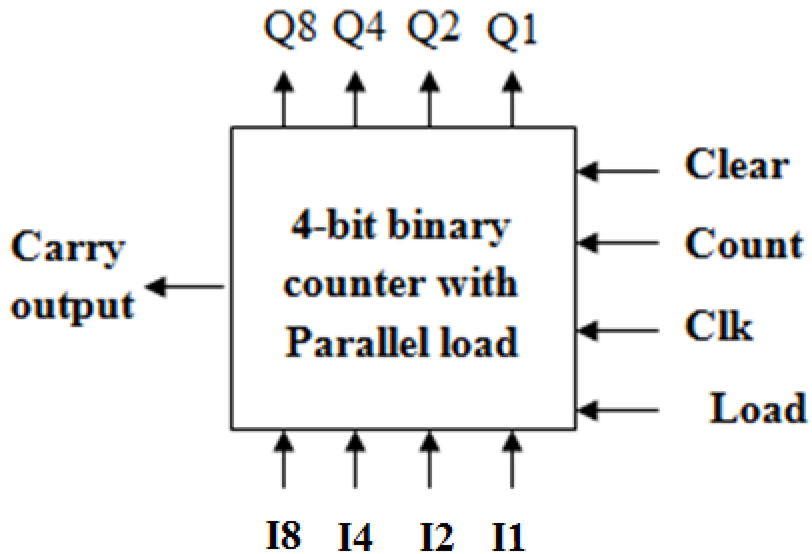


Clear	Clk	Load	Count	Function
0	X	X	X	Clear all
1	↑	1	X	Load input
1	↑	0	1	count
1	↑	0	0	No change

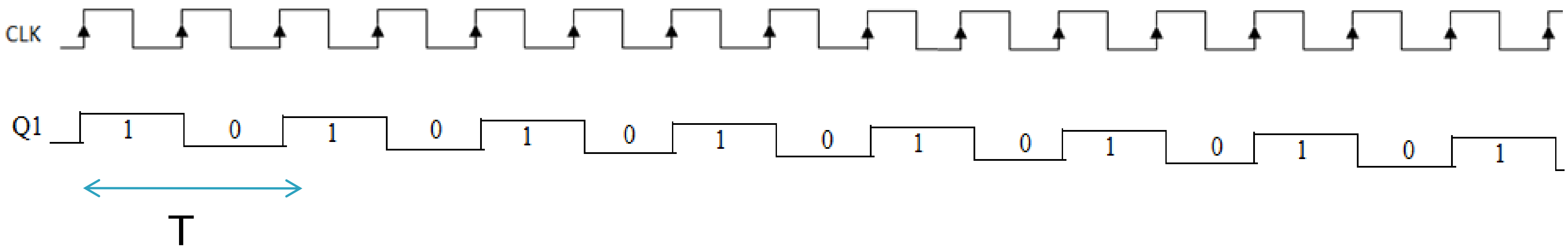
Programmable counters



Frequency division (F/n)



Frequency division (power of 2)

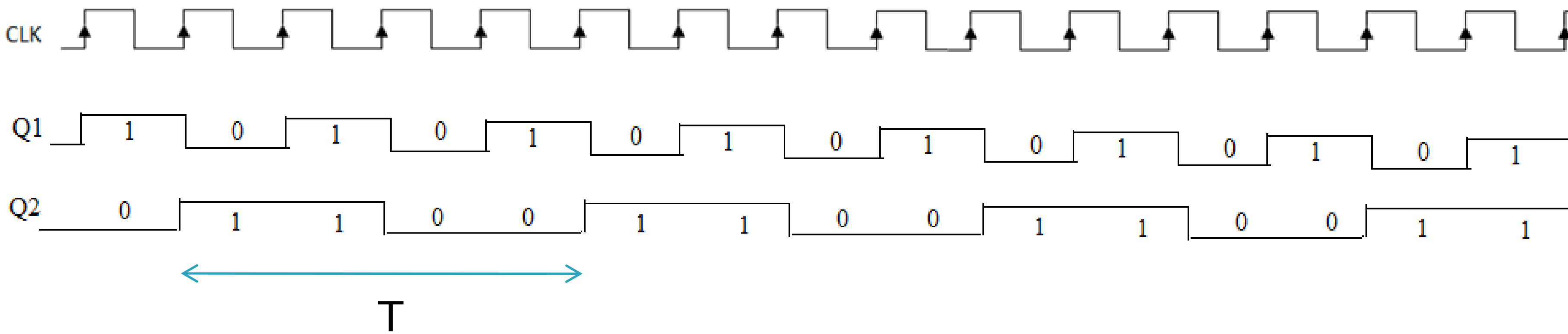


$$T_{Q1} = 2\,T_{clk}$$

$$F_{Q1} = 1/\,2\,T_{clk}$$

$$F_{Q1} = F_{clk}/\,2$$

Frequency division (power of 2)

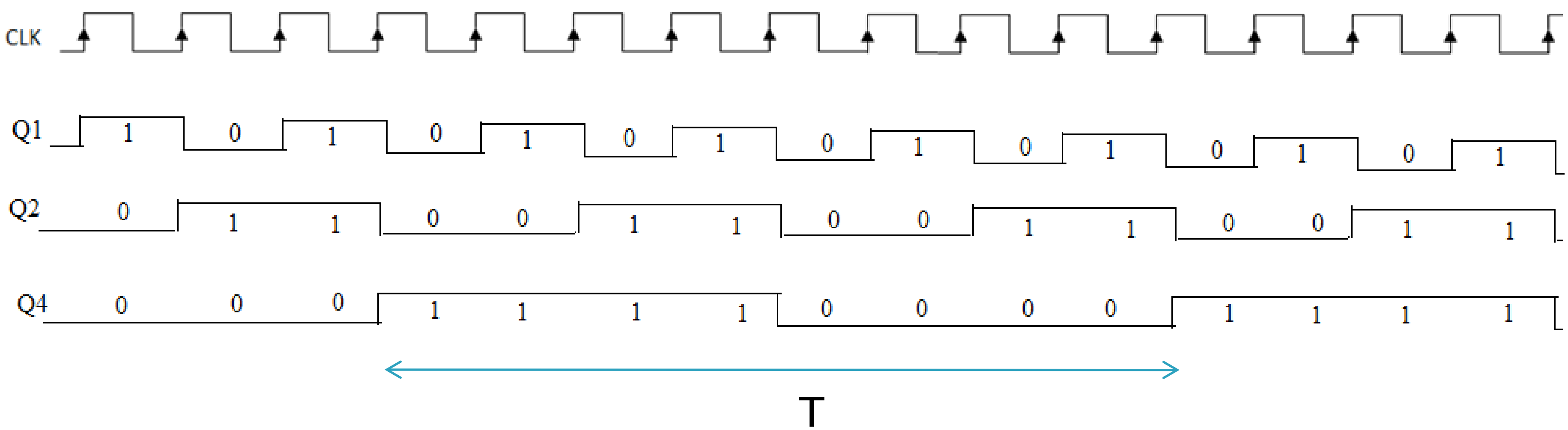


$$T_{Q2} = 4\ T_{clk}$$

$$F_{Q2} = 1 / 4\ T_{clk}$$

$$F_{Q2} = F_{clk} / 4$$

Frequency division (power of 2)

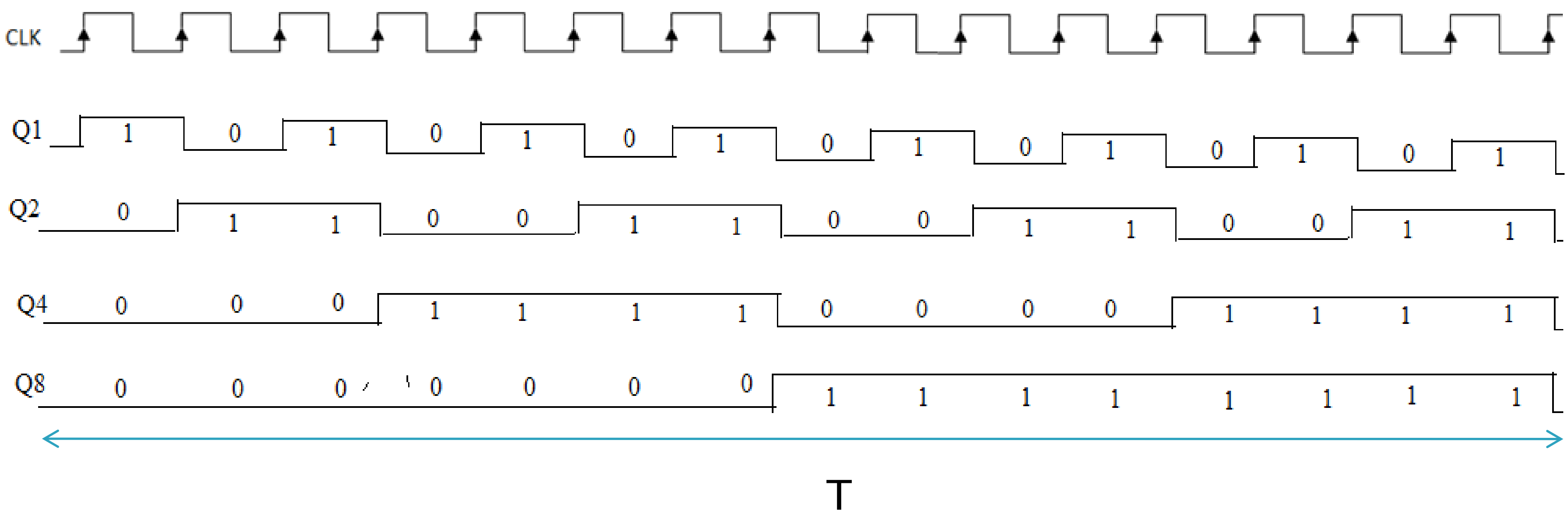


$$T_{Q4} = 8\ T_{clk}$$

$$F_{Q4} = 1/\ 8\ T_{clk}$$

$$F_{Q4} = F_{clk}/\ 8$$

Frequency division (power of 2)

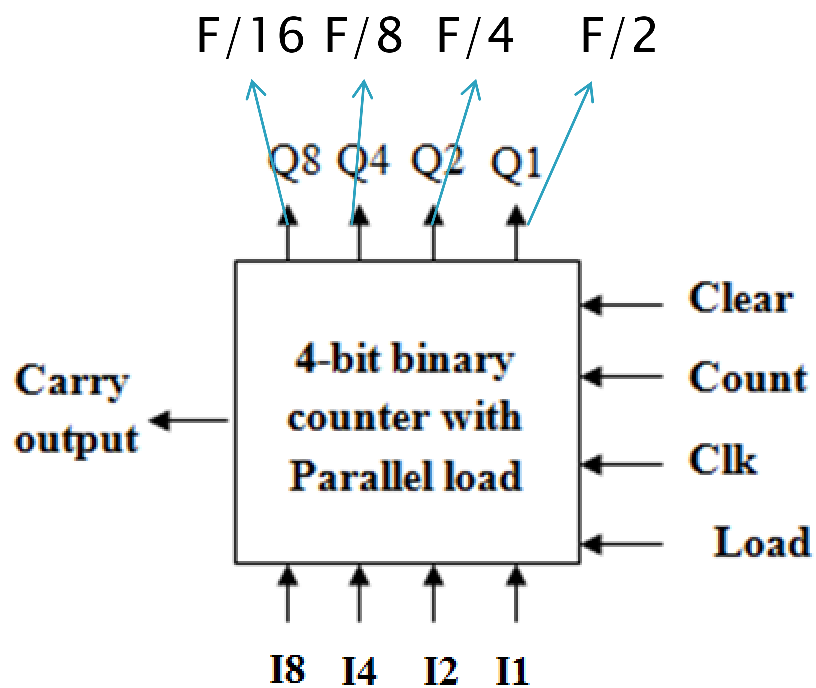


$$T_{Q8} = 16\ T_{clk}$$

$$F_{Q8} = 1/\ 16\ T_{clk}$$

$$F_{Q8} = F_{clk}/\ 16$$

Frequency division (power of 2)



Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the beginning (using load)

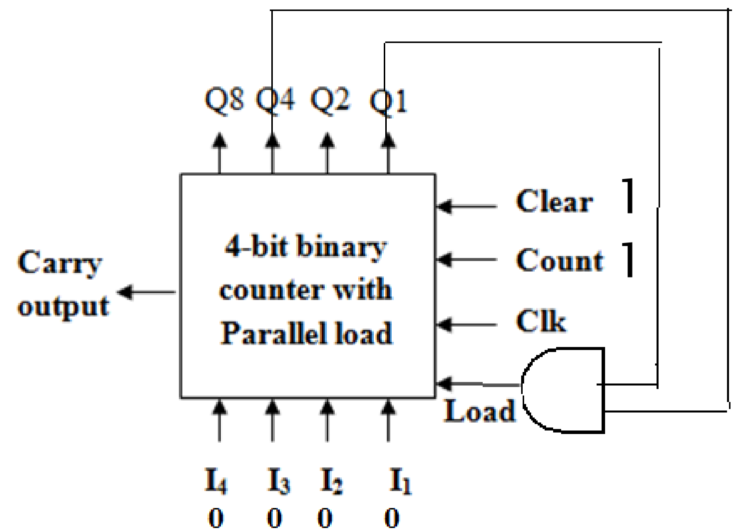
Q8	Q4	Q2	Q1	load
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1

Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

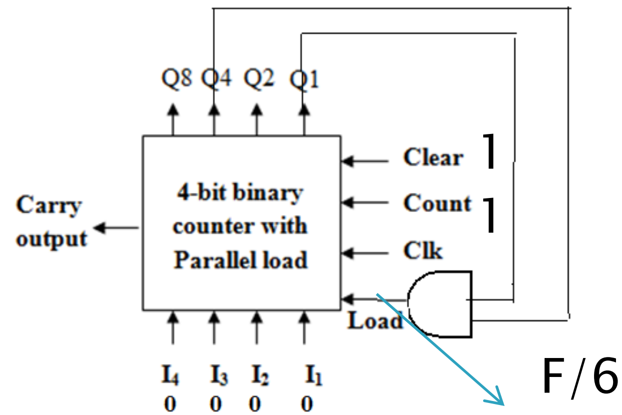
From the beginning (using load)

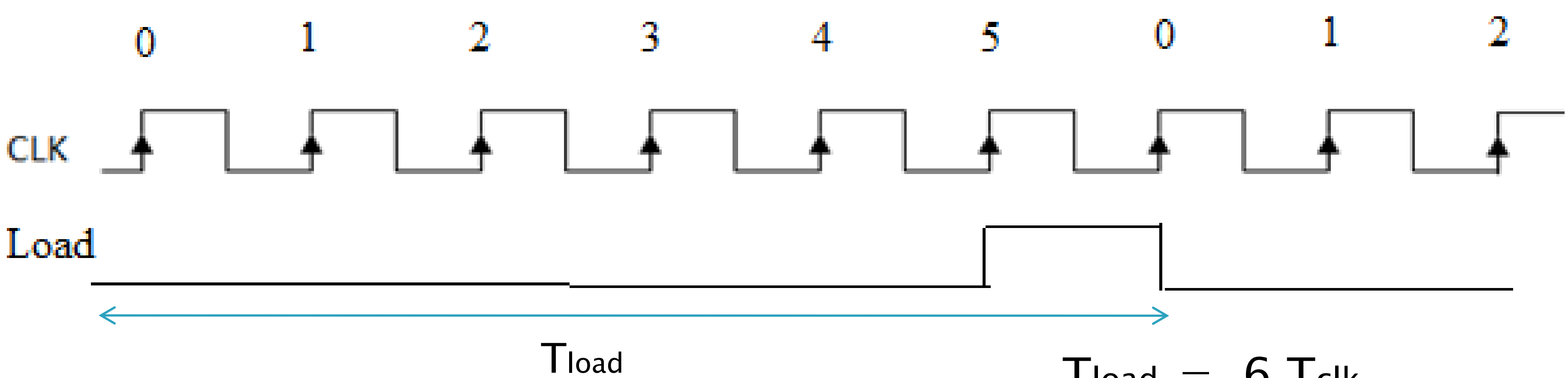
Q8	Q4	Q2	Q1	load
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1



Frequency division (F/6)

Q8	Q4	Q2	Q1	load
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1





$$T_{load} = 6\,T_{clk}$$

$$F_{load} = 1/\,6\,T_{clk}$$

$$F_{load} = F_{clk}/\,6$$

Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the beginning (using clear)

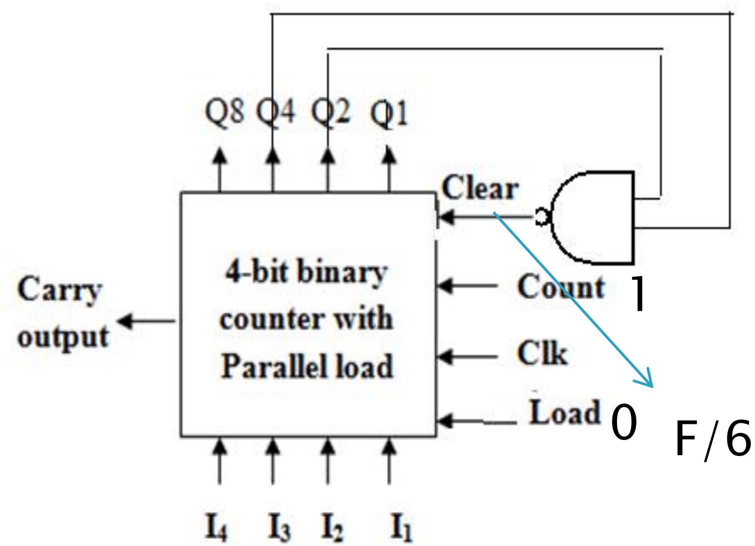
Q8	Q4	Q2	Q1	clear
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0

Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the beginning (using clear)

Q8	Q4	Q2	Q1	clear
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0



Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the middle

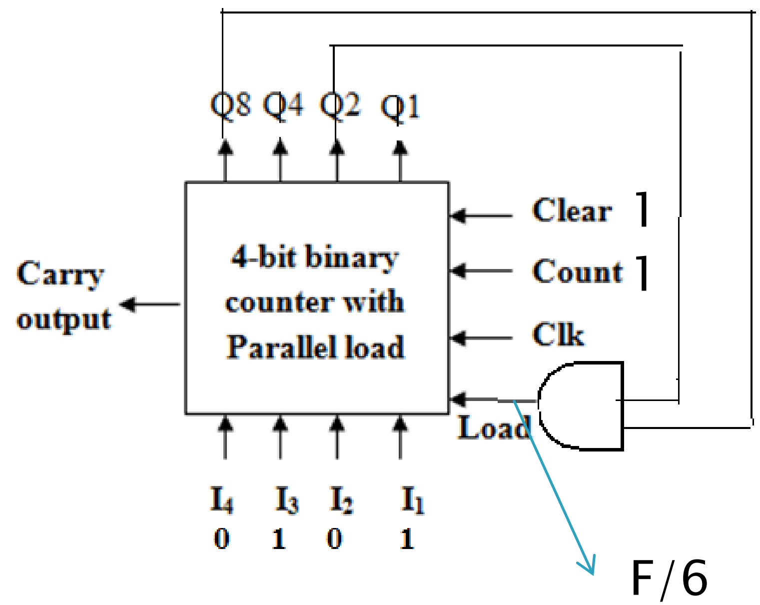
Q8	Q4	Q2	Q1	load
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1

Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the middle

Q8	Q4	Q2	Q1	load
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1



Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the end

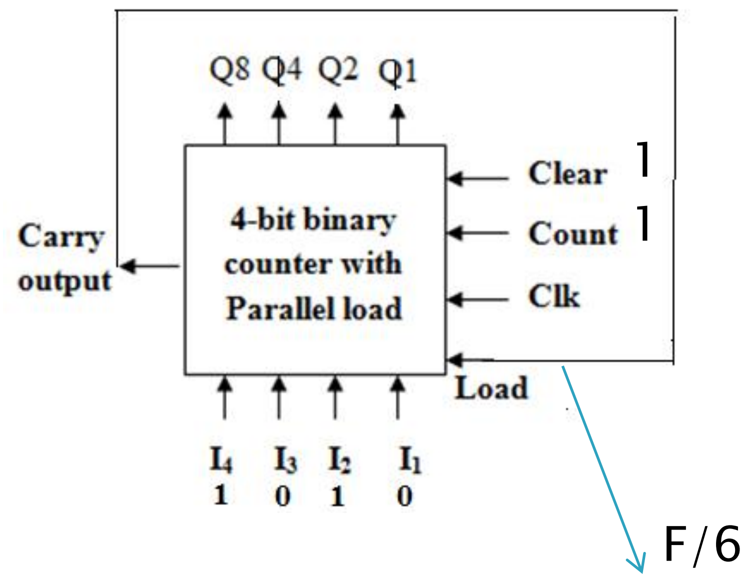
Q8	Q4	Q2	Q1	load
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Frequency division (F/n)

- Counter mod n
- Ex: n= 6 to get f/6

From the end

Q8	Q4	Q2	Q1	load
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



Next Lecture we will explain Computer Memories

Thank you